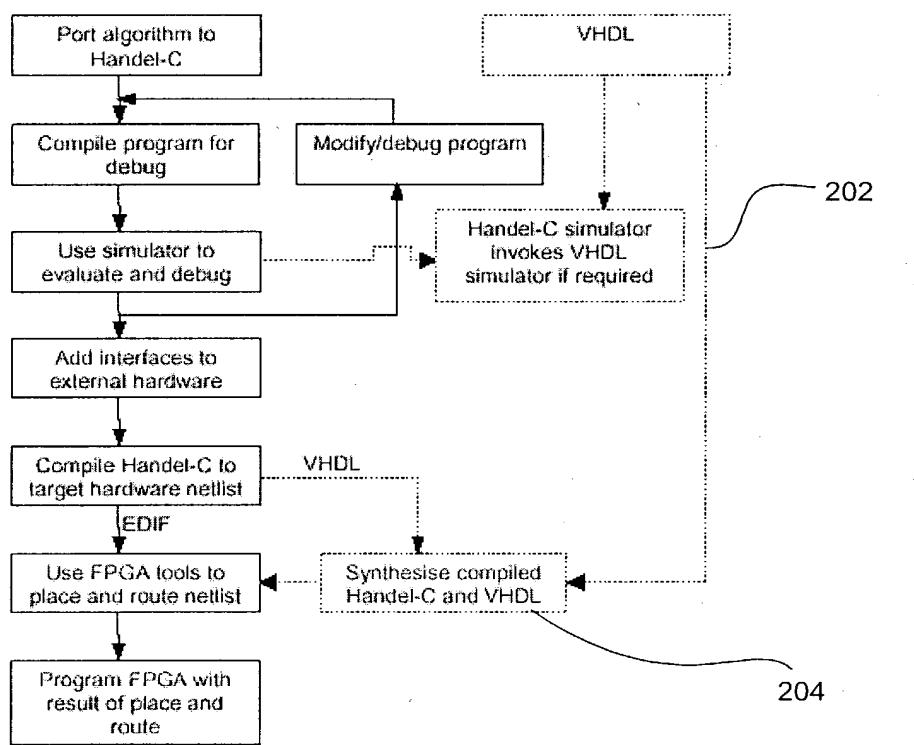


Fig. 1



**FIG. 2**

<b>Workspace window</b>	The area where you organise your projects. A project consists of all the files you need, plus information about what target you are compiling for. When you have assembled all the information that you need for a project, you can compile it. When you start Handel-C, the default position of the workspace window is on the left.
<b>Code editor</b>	Where you create and edit Handel-C source files. When you create or open a file, the default position of the code editor window is on the right.
<b>Output window</b>	When you compile a file, error messages and warnings are displayed in the output window. The default position of the output window is at the bottom of the screen. The output window has tabs for build messages and debug messages.
<b>Debug windows</b>	When your file has compiled, you can simulate it. The simulation steps the program through clock cycles, and allows you to look at the contents of any variables that are in scope. These are displayed in the <b>Variables</b> window.  You can select variables to display in the debug <b>Watch</b> window. The default position of the watch window is the bottom left-hand corner of the screen. The call stack (the route by which you have called a function) is displayed in the <b>Call Stack</b> window.  You can see clock cycles in the <b>Clocks</b> window and current executing threads in the <b>Threads</b> window

FIG. 3

400

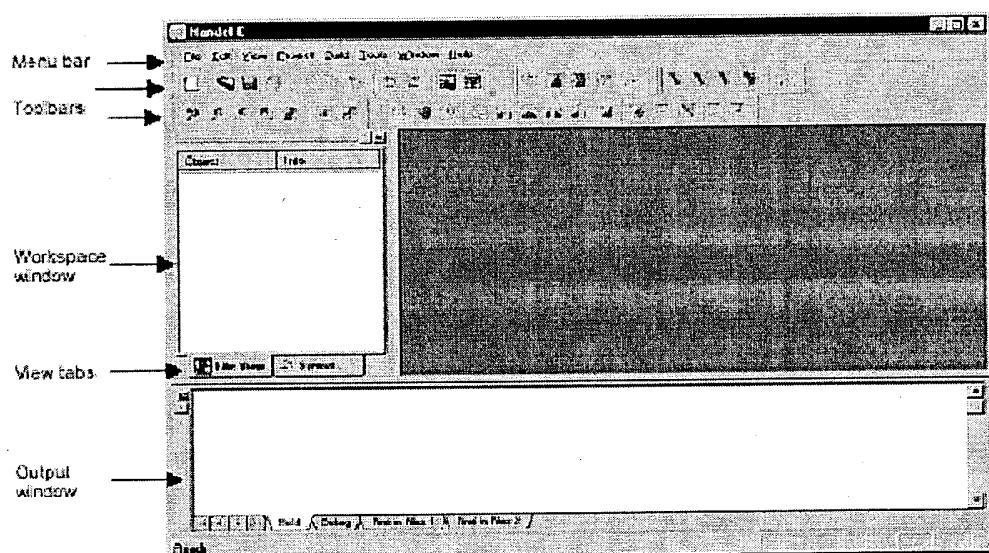
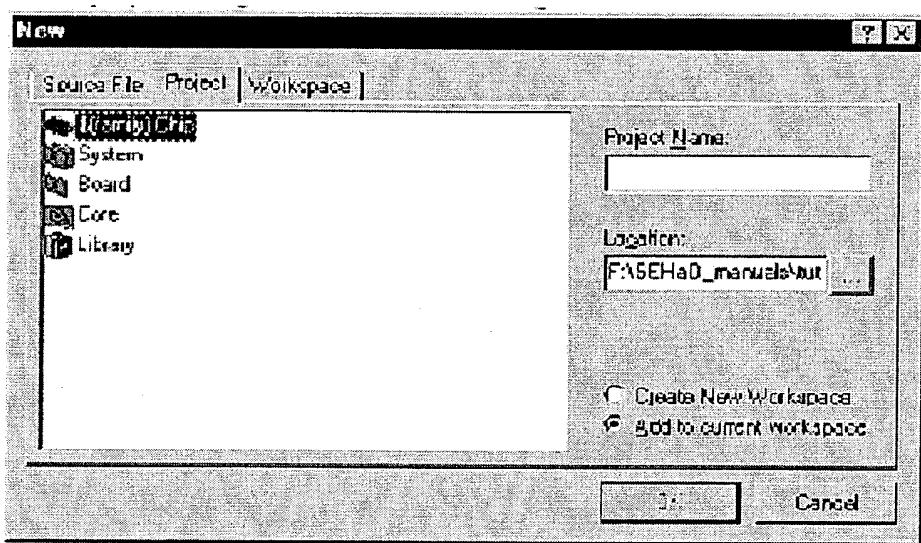


FIG. 4

500



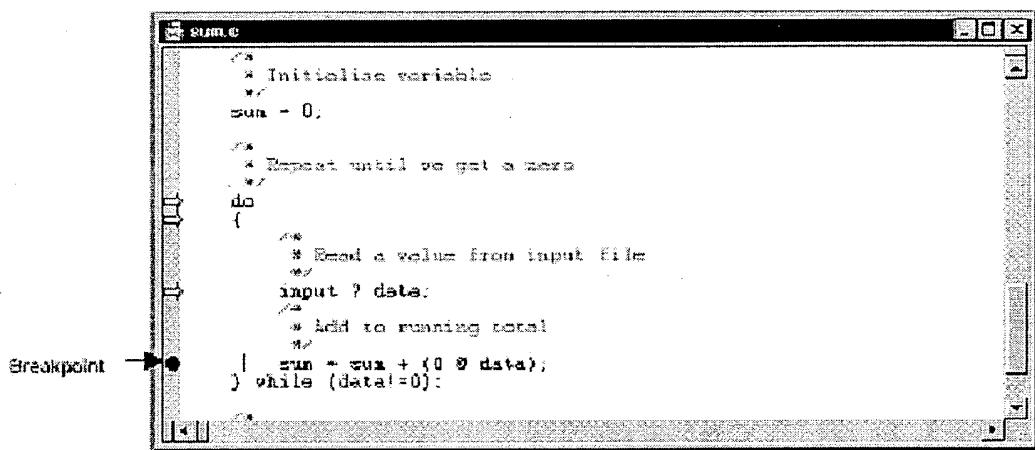
**FIG. 5**

600

a chip <sup>600</sup> , system <sup>600</sup> or board <sup>600</sup>	Not targeted to a particular system or product
a core <sup>600</sup>	A discrete piece of code, compiled to a specific architecture, that may be used as part of a larger design
a library <sup>600</sup>	Pre-compiled Handel-C code that may be re-used or sold elsewhere
a pre-defined chip, system or board	Targeted to a known product. These systems will be optimised for that product, and should only be placed and routed onto that product.

**FIG. 6**

700



```
sum.c
/*
 * Initialise variable
 */
sum = 0;

/*
 * Repeat until we get a zero
 */
do
{
    /*
     * Read a value from input file
     */
    input ? data;
    /*
     * Add to running total
     */
    sum = sum + (0 & data);
} while (data!=0);
```

FIG. 7

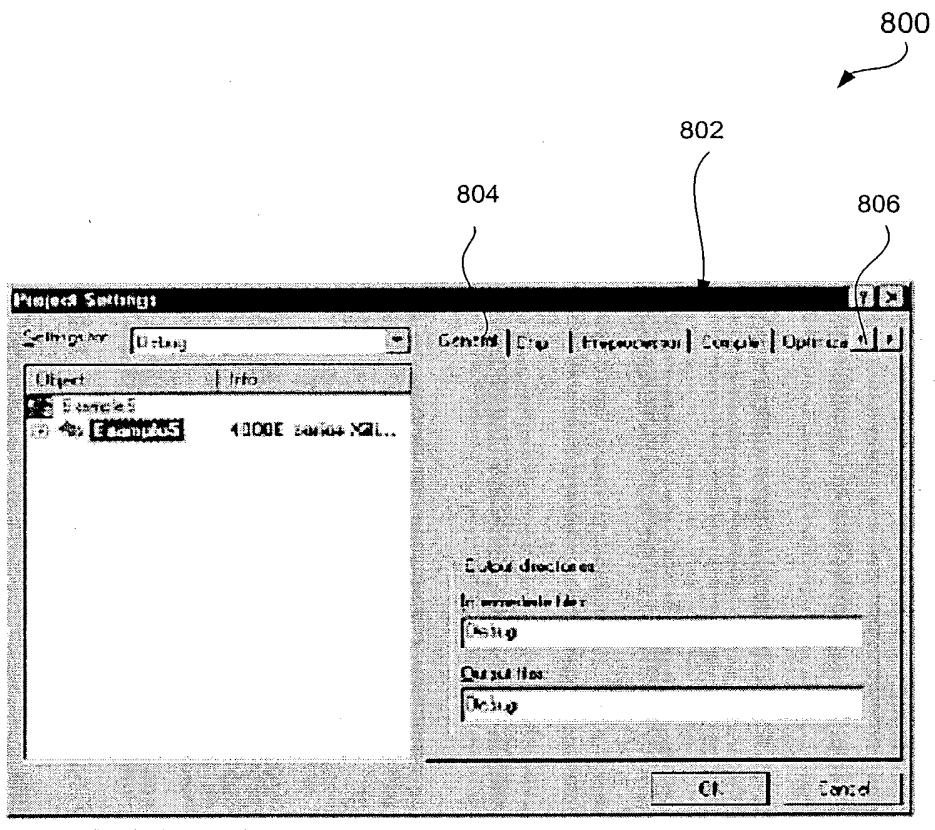


FIG. 8

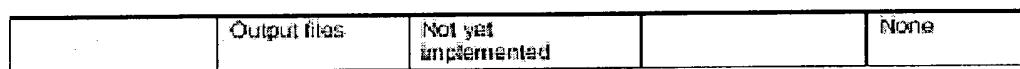
Tab	Item	Meaning	Value	Default
<b>General</b>				
	Intermediate files	The sub-directory where intermediate files are stored	Directory path name relative to the project directory	configuration name
	Output files	The sub-directory where the final output is stored (.d11, netlist etc.)	Directory path name relative to the project directory	configuration name
<b>Chip</b>				
	Family	The family containing the part you are targeting	Select family from drop-down list	As required
	Part	The part number you are targeting	Type in part number	Depends on project

FIG. 9A

Preprocessor				
	Preprocessor definitions (-D)	Equivalent to the #define directive	Set as required	DEBUG, NDEBUG, SIMULATE
	Additional include directories (-I)	Add directories to the search path for include directories	Set as required	None
	Additional preprocessor options (-cpp)	Add any cpp commands	See the pre-processor manual	None
Compiler				
	Generate debug information (-g)	Get the compiler to produce information for the debugger	Check for Yes	Checked
	Generate warning messages (-W)	Get the compiler to produce warning messages	Check for Yes	Checked
	Generate estimation information (-e)	Get the compiler to generate HTML files giving depth and timing information	Check for Yes	Unchecked
Optimisations				
	Various levels of optimizations	Check as needed	Depends on target	
Linker				
	Output format	Select the target for the compiler	Determined by target settings	As required
	Save browse info	Store information needed to browse symbols	Checked	Checked
	Additional Library Path	Directory path to search for libraries	Set as required	
	Command line for building simulator DLL (-cl)	Link options defined in the cl.cf file	Define how the C compiler is called to compile simulator .dll	Installed cl.cf settings. (Debug and Release only)
	Object/library modules	Specify modules to include in build	Set as required	
Debugger				
	Working directory	Directory that the simulator uses as the current working directory	Directory path name relative to the project directory	Defaults to current project directory (.)
Build commands				
	Compilation commands	Not yet implemented		None

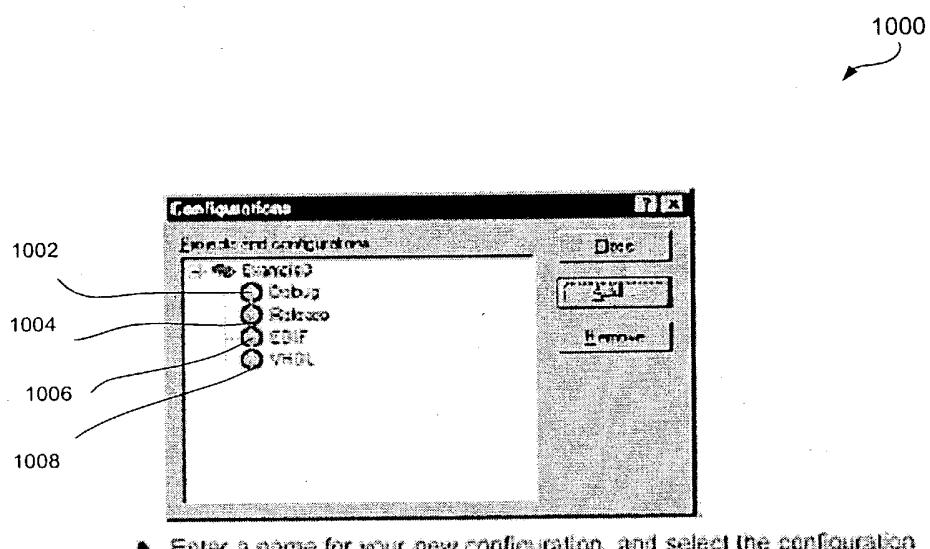
FIG. 9B

900

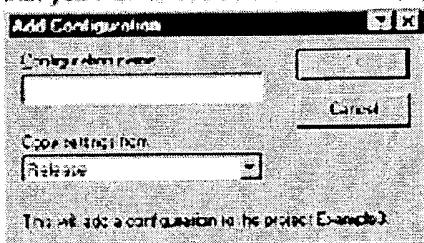


	Output files	Not yet implemented	None
--	--------------	---------------------	------

**FIG. 9C**



- Enter a name for your new configuration, and select the configuration type that you wish to use as a base in the **Copy settings from** box.



**FIG. 10**

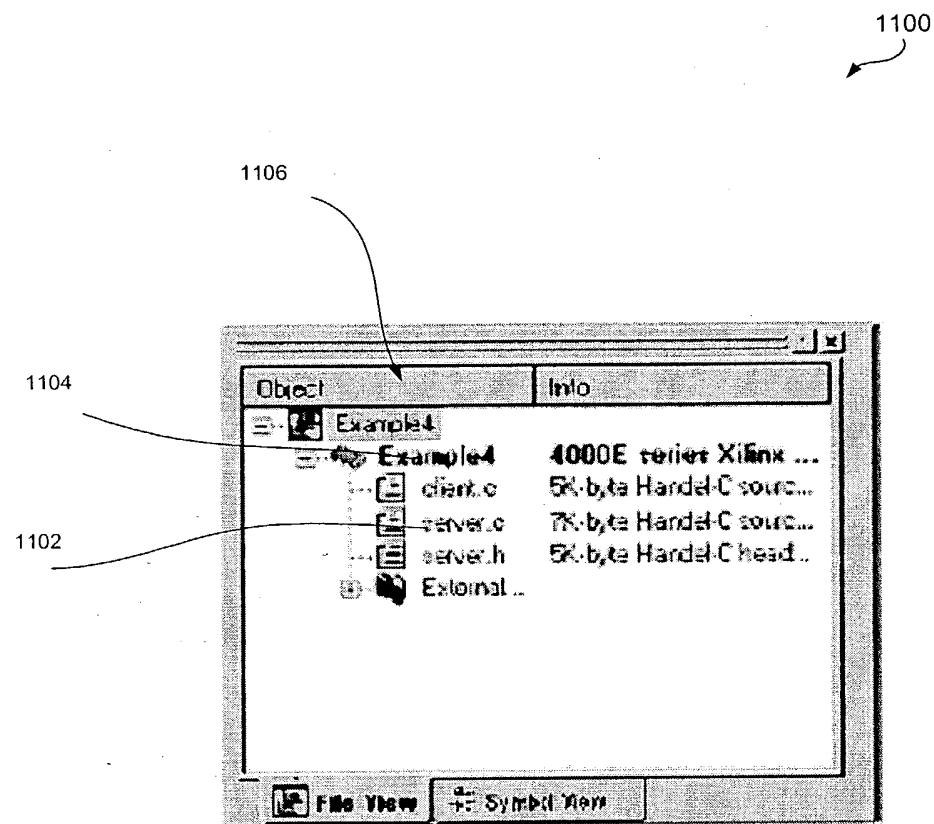
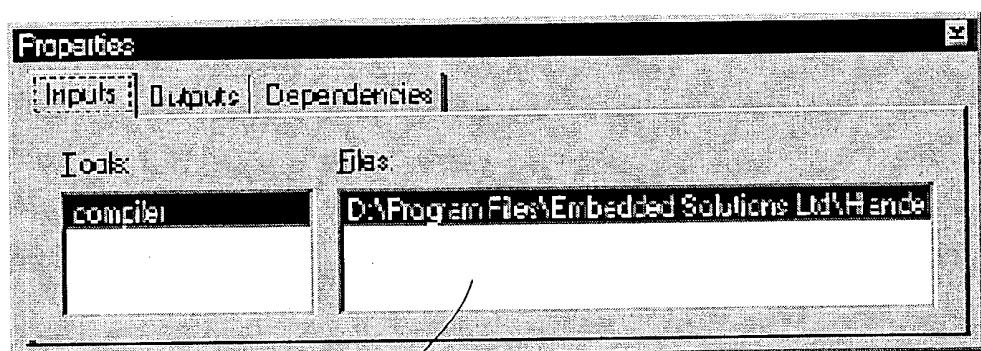


FIG. 11

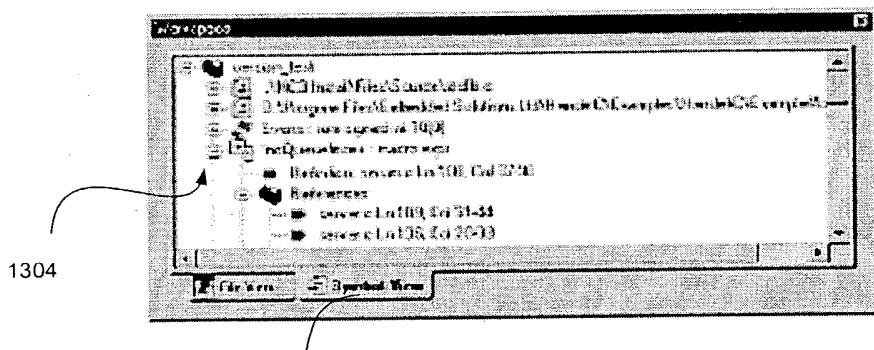
1200



1202

FIG. 12

Icon	Meaning
█	shared function, procedure or expression
█	in-line function or macro
●	variable
█	memory (RAM, ROM, WOM or MPRAM)
█	channel
█	external interface
█	signal
█	Stacked positions that contain the related object (e.g. recursive macros)
█	Position in the file containing the definition of the object



**FIG. 13**

1400

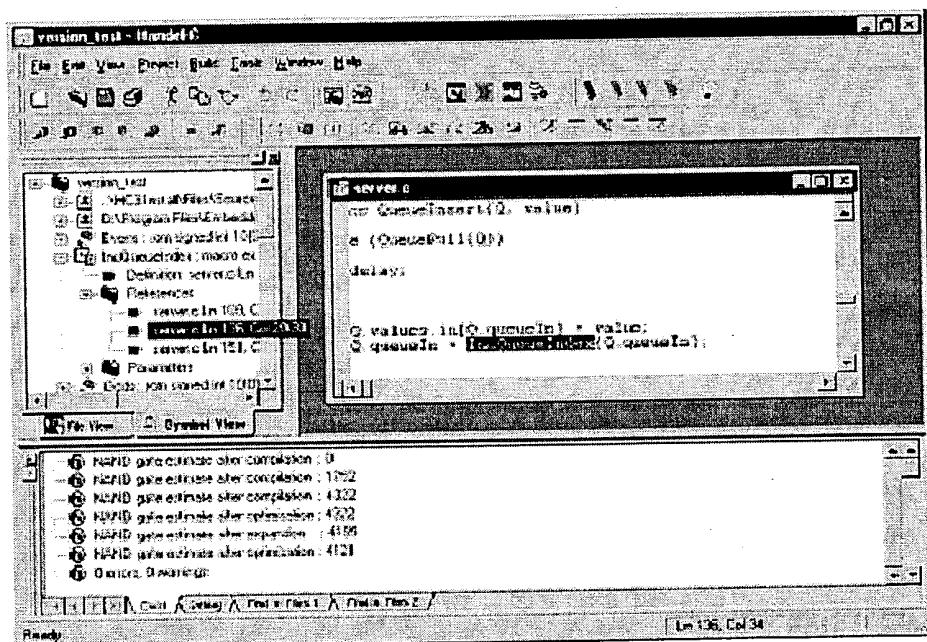
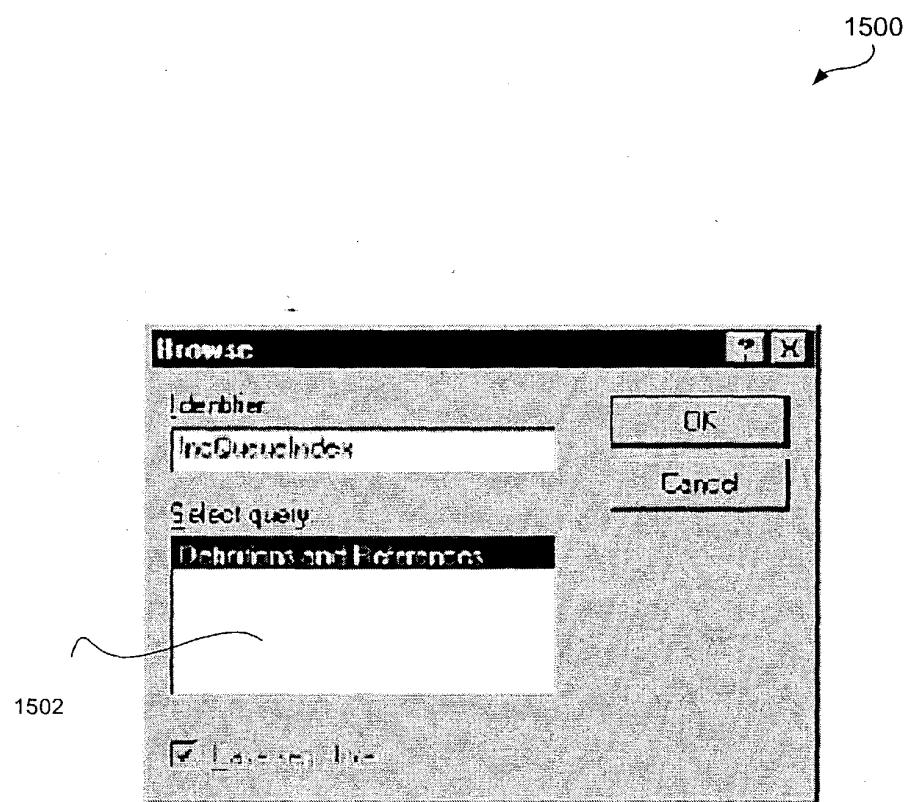


FIG. 14



**FIG. 15**

1600

### Browsing

Button	Command	Function
1	Go to Definition	Jump to the source code line where the variable is defined
2	Go to Reference	Jump to the first source code line where the variable is used
3	Previous Definition/Reference	Jump to previous definition or reference

FIG. 16A

1600



	<b>Next Definition/Reference</b>	Jump to next definition or reference
	<b>Pop context</b>	Returns you to your original position before you started browsing

**FIG. 16B**

Command	Shortcut	Function
<b>Undo</b>	Ctrl+Z	Reverse a recent change to the active document or to the workspace
<b>Redo</b>	Ctrl+Y	Reverse a recent undo
<b>Cut</b>	Ctrl+X	Copy the current selection and delete it
<b>Copy</b>	Ctrl+C	Copy the current selection to the clipboard
<b>Paste</b>	Ctrl+V	Copy the clipboard to the current selection
<b>Delete</b>	Del	Delete the current selection
<b>Find</b>	Ctrl+F	Find a string or regular expression in the current file
<b>Find in Files</b>		Find a string or regular expression in selected files
<b>Replace</b>	Ctrl+H	Replace one string or regular expression with another in current file

The **Edit** menu also has the **Bookmarks** and **Browse** sub-menus and the **Breakpoints** command.

**FIG. 17**

Regular Expression	Description
(x)	The characters or expressions between the parentheses
.	(Period.) Any single character.
^	Start of line.
\$	End of line.
\t	Tab character
x y	A match for either x or y. For example, a(team class) will match either ateam or aclass.
x*	Zero, one or many copies of x. For example, ba*c matches bac, baac, baaac and bc.
x?	None or one x. For example, ba?c matches bac or bc.
x+	At least one or more of x. For example, ba+c matches bac, baac, baaac, but not bc.
[xyz] [x-y]	Matches one character from the set in the brackets. Use a dash (-) to include all characters in a range (e.g., [A-Za-z] matches an underscore or any letter, and [A-Za-z][A-Za-z0-9]* matches an alphanumeric string that can include underscores). Use [xyz-] or [-xyz] if you want to include a dash in the set. If you need a ] in the set use []xyz].
[^xyz]	Matches one character that is not in the brackets. For example, x[^0-9] matches xa, but not x0 or x2.
\x	Matches the character x, even if x is one of the magic characters ^\$[], *? listed above. For example, ^pig matches pig at the start of a line, but \^pig matches the string ^pig anywhere on a line.

FIG. 18

1900

Directory	File	File type
Where saved	prog.c	Source file
Workspace directory	prog.hw	Workspace
Project directory	example1.hp	Your project file
Output directory	example1.dll	Part of the simulator
	example1.lib	Part of the simulator
	example1.hb	The project browse file for the symbol view window
	example1.exp	Part of the simulator
	prog.hb	A program browse file used for symbol view
Intermediate directory	prog.obj	Handel-C object file built during compilation.

**FIG. 19**

more and more people are using the Internet to buy and sell items online. This is because it is a quick and easy way to sell products without having to leave their home.

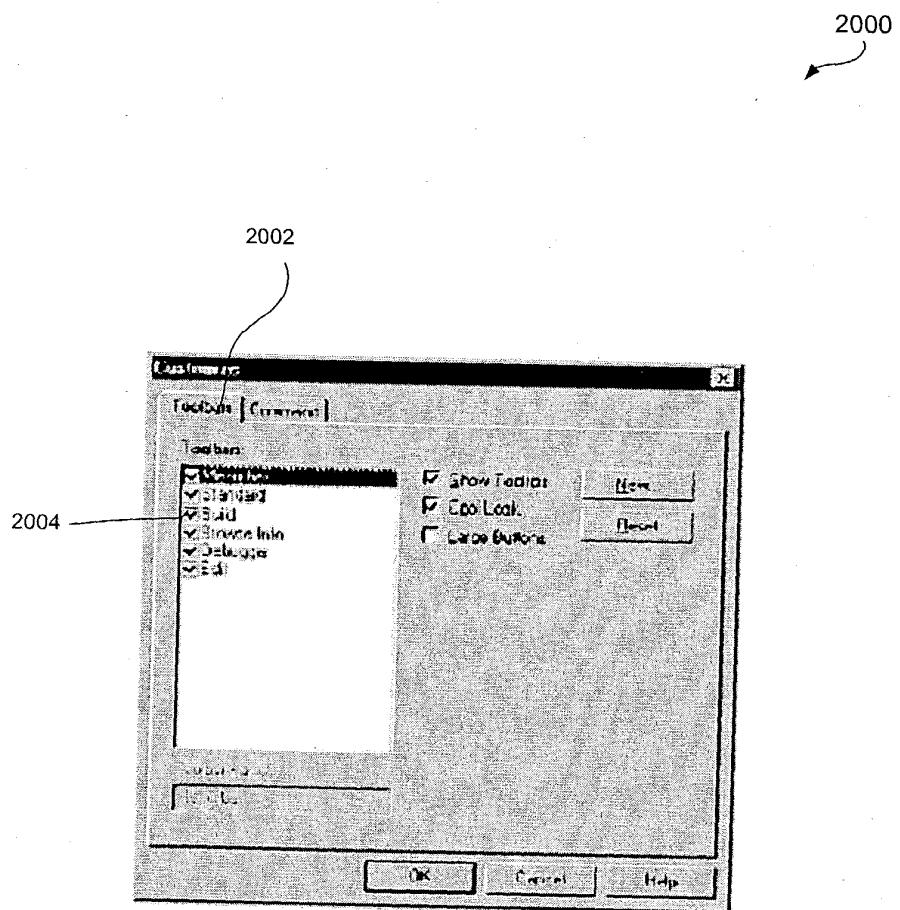


FIG. 20

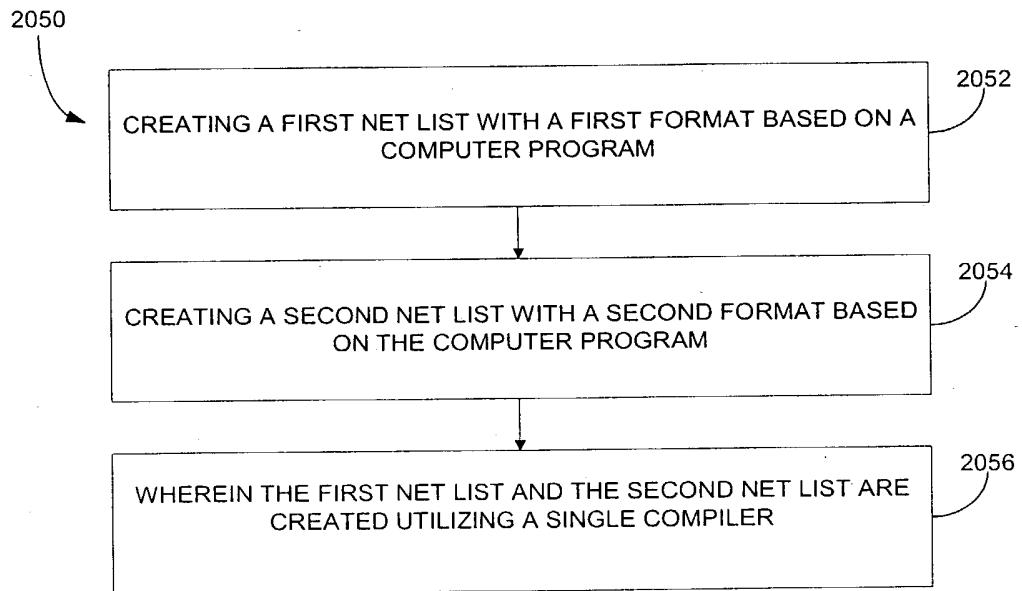
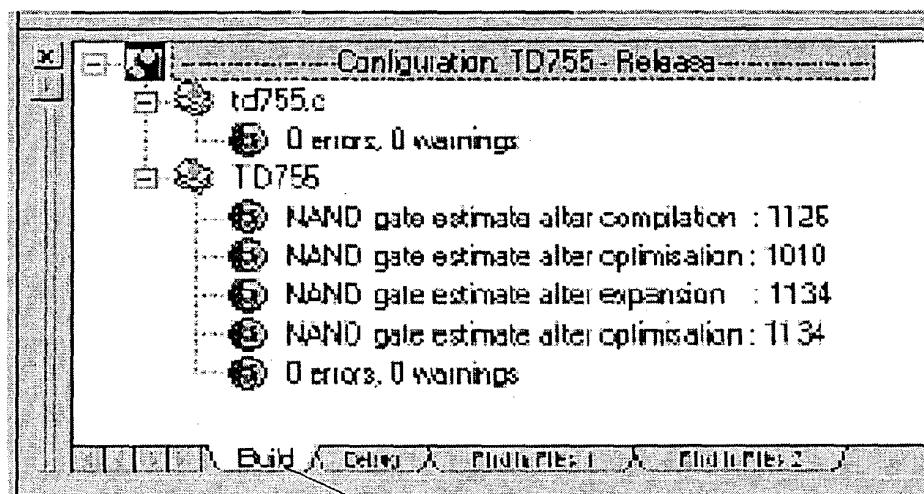


Fig. 20A

2100



2102

**FIG. 21**

Command	Shortcut	Function
<b>Compile</b>	Ctrl+F7	Run the compiler on the active document (which must be a .c file), to generate its .obj file.
<b>Build project</b>	F7	Build this project: Run the compiler on all .c files that are newer than their .obj files, then run the linker on the .obj files to make the .d11, EDIF or VHDL file.
<b>Rebuild All</b>		Rebuild all the files in this project like Build, except that all .c files are compiled.
<b>Clean</b>		Delete all the files that are created by Build.
<b>Start Debug</b>		Pop-up menu
<b>Go</b>	F5	(Build project if not built.) Run the simulator at full speed (until a breakpoint or other stop is reached)
<b>Step Into</b>	F11	(Build project if not built.) Run to the first statement in the function or macro invoked in the current line. If the current line is not a function or macro invocation, run to the next statement.
<b>Run to Cursor</b>	Ctrl+F1	(Build project if not built.) Run up to the line containing the text cursor.
<b>Set Active Configuration</b>		Shows a dialogue box where the user can choose the active configuration
<b>Configurations...</b>		Shows a dialogue box where the user can add, remove or edit configurations.

FIG. 22

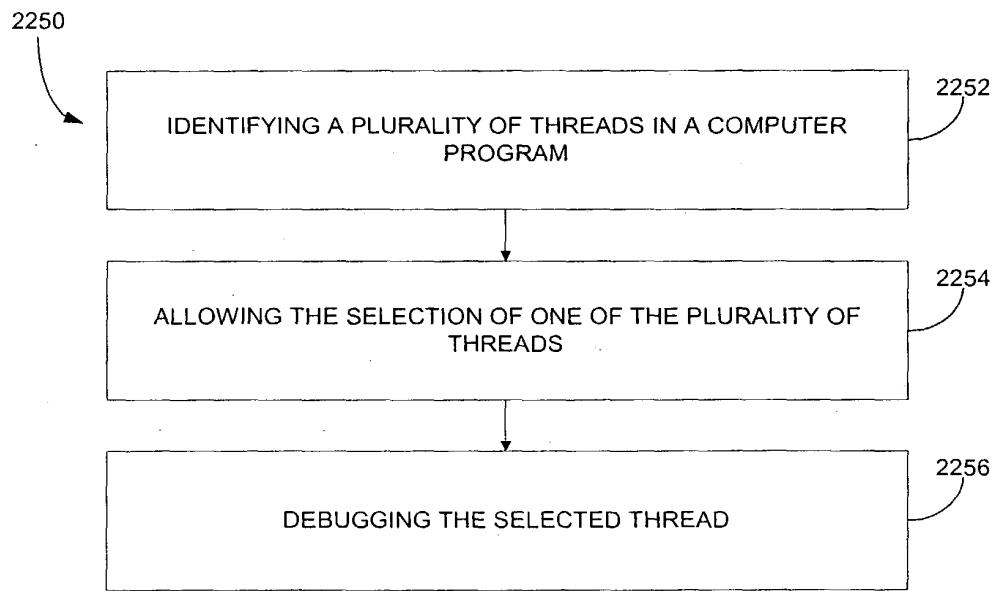


Fig. 22A

2300

Command	Shortcut	Function
Go	F5	Run the simulator at full speed (until a breakpoint or other stop)
Restart	Ctrl+Shift+F5	Run the simulator, starting at the first line of the program.
Stop Debugging	Shift+F5	Stop the simulation
Break		Pause the simulation (when it is running)
Show Next Statement	ALT + keypad *	Display the statement in the current thread that will be executed on the next clock cycle
Step Into	F11	Run to the first statement in the function invoked in the current line. If the current line is not a function invocation, run to the next statement on a complete clock cycle.
Step Over	F10	Run until the start of the next statement (step over a function)
Step Out	Shift+F11	Run until the start of the statement after the line which invoked the current function (step out of a function)

**FIG. 23A**

2300

<b>Run to Cursor</b>	Ctrl+F10	Run until the line containing the text cursor is reached.
<b>Advance</b>	Ctrl+F11	Advance a partial clock cycle, to the next code line

**FIG. 23B**

2400

Window	Shortcut to open	Function
Editor window	Appears by default	The code editor window for the source code that you are debugging, marked to show the current execution points and breakpoints.
Watch	Alt+9	A window with four tabs, in which you can view the contents of selected variables.
Call Stack	Alt+F7	A window that shows the calling path to the function you are in.
Variables	Alt+4	Variables window.
Clocks	Alt+9	Displays all current clocks and their values.
Threads	Alt+5	Displays all current threads with a unique identifier, and allows you to select one to view.

FIG. 24

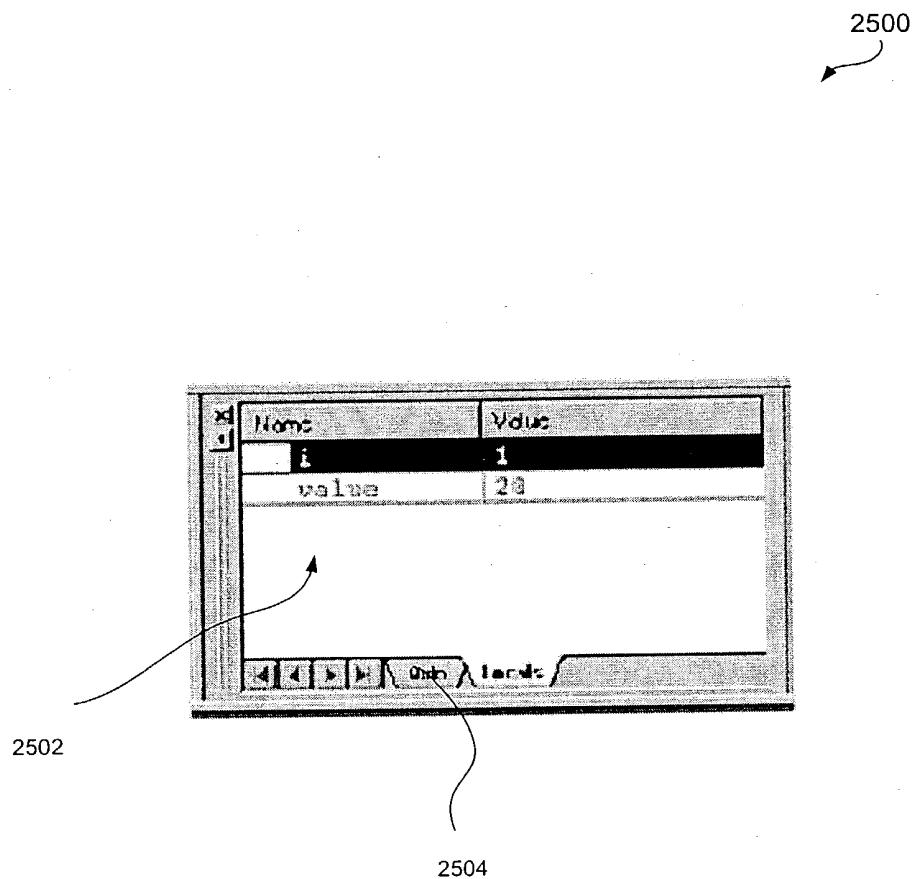
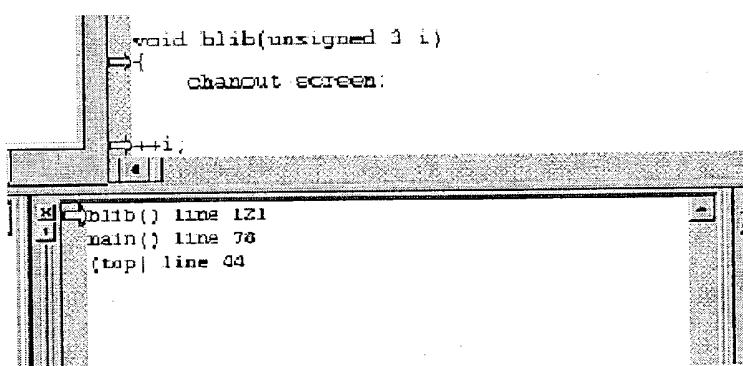


FIG. 25

2600



void blib(unsigned i)  
{  
 chanout screen;  
  
 i++;  
}

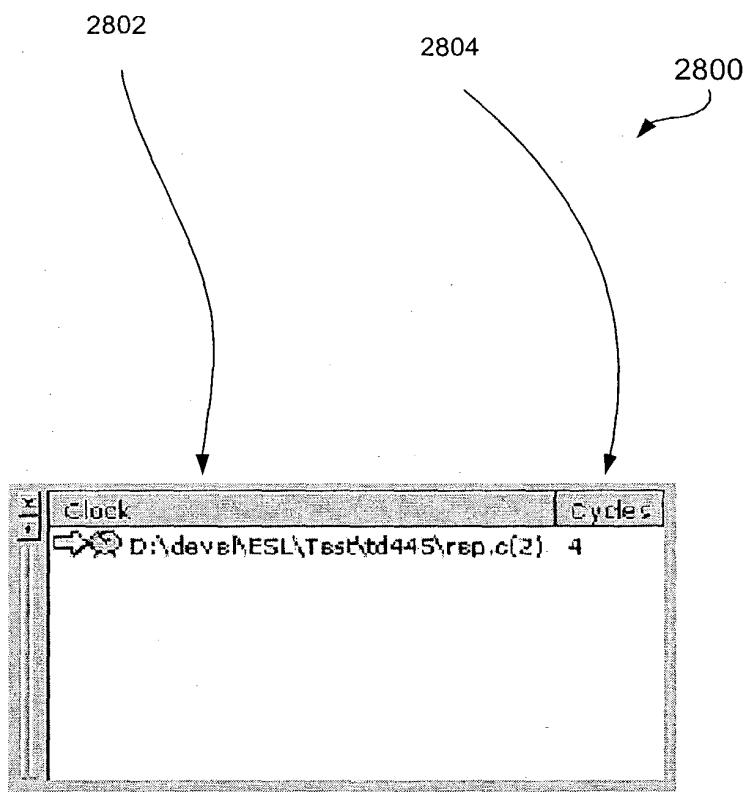
blib() line 121  
main() line 78  
{tmp| line 44

**FIG. 26**

Handwritten labels: 2702, 2704, 2706, 2708, 2700

Thread	State	Location
2702	producer()	main.c(58)
2703	car (i=6) in main()	queue.o(74)
2704	consumer()	main.c(79)
2705	car (i=1) in main()	queue.o(74)
2706	car (i=2) in main()	queue.o(74)
2708	car (i=3) in main()	queue.o(74)

FIG. 27



**FIG. 28**

2900

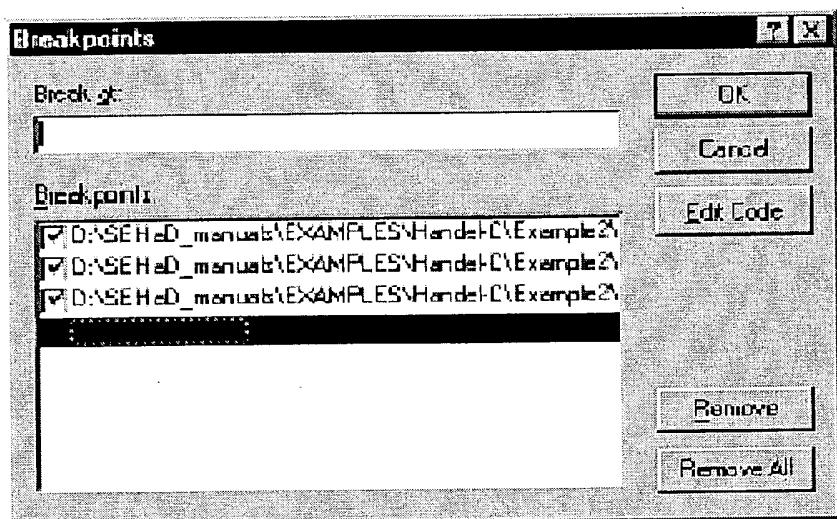


FIG. 29

Strong typing	Handel-C has variables which can be defined to be of any width.
	Casting can't change width.
	There are no automatic conversions between signed and unsigned values. Instead, values must be 'cast' between types to ensure that the programmer is aware that a conversion is occurring that may alter the meaning of a value.
	Pointers can only be cast to <code>void</code> and back, between <code>signed</code> and <code>unsigned</code> and between similar <code>structs</code> . You cannot cast pointers to any other type
True parallelism	You can have multiple main functions in a project. Each Handel-C main function must be associated with a clock.
	Although implicitly sequential, Handel-C has parallel constructs which allow you to speed up your code
Width of variables	Handel-C has variables which can be defined to be of any width.
	In ISO-C, bit fields are made up of words, and only the specified bits are accessed, the rest are padded. Since there are no words in Handel-C, no form of packing can be assumed.
	If you have an <code>array[4]</code> and you use its index as a counter, the index width will be assumed by the Handel-C compiler to be two bits wide (to hold the values 0 – 3). It will not be able to hold the value 4.
No side-effects allowed	Instead of writing complex single statements, it is more efficient in Handel-C to write multiple single statements and run them in parallel
	You cannot perform two assignments in one statement.
	<code>auto</code> variables cannot be initialised, as that means that hidden clock cycles are required. Instead, they must be explicitly assigned to in a separate statement.

FIG. 30

3100

	You cannot have empty loops in Handel-C
Constrained functions	Functions may not be recursive.
	Variable length parameter lists are not supported.
	Old-style function declarations are not supported.

**FIG. 31**

3200

In Both	In Conventional C Only	In Handel-C Only
int	double	chan
unsigned	float	ram
char	union	rom
long		wom
short		mpram
enum		signal
register		chanin
static		chanout
extern		undefined
struct		interface
volatile		<>
void		inline
const		typeof
auto		
signed		
sizeof		
void		
volatile		

FIG. 32

3300

In Both	In Conventional C Only	In Handel-C Only
( ; )		par
switch		delay
do ... while		?
while		!
if ... else		parallel
for ( ; ; )		seq
break		ifselect
continue		
return		
goto		
assert		

**FIG. 33**

3400

FIG. 34

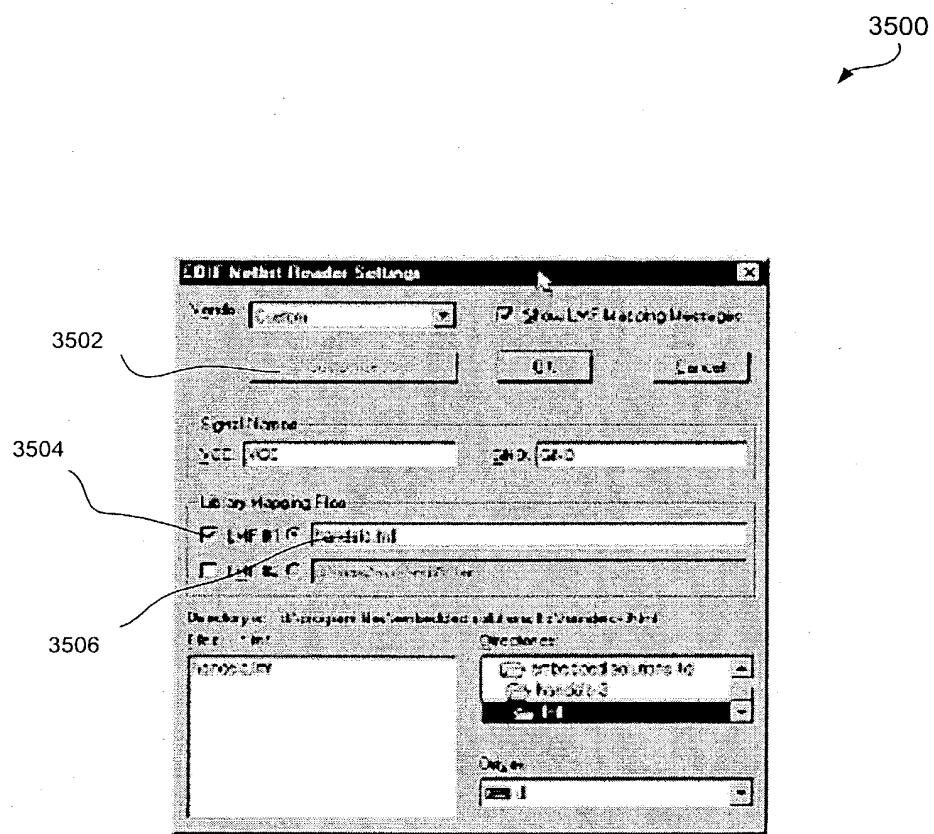
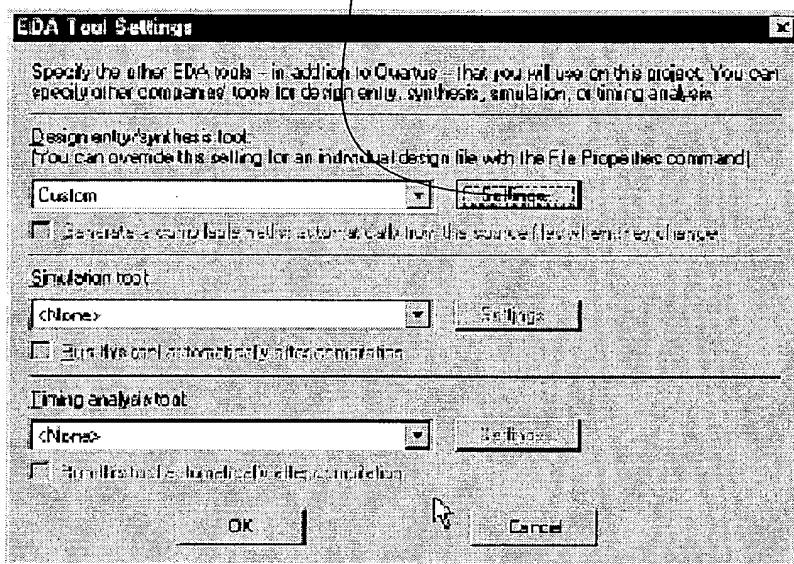


FIG. 35

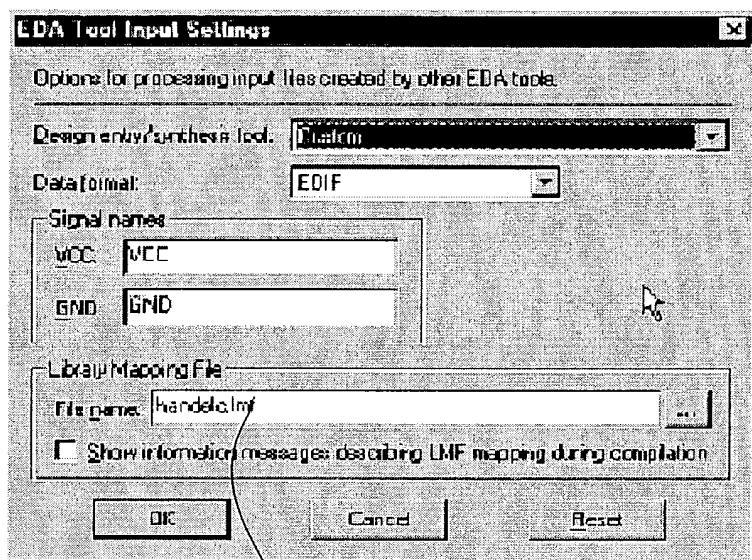
3602

3600



**FIG. 36**

3700



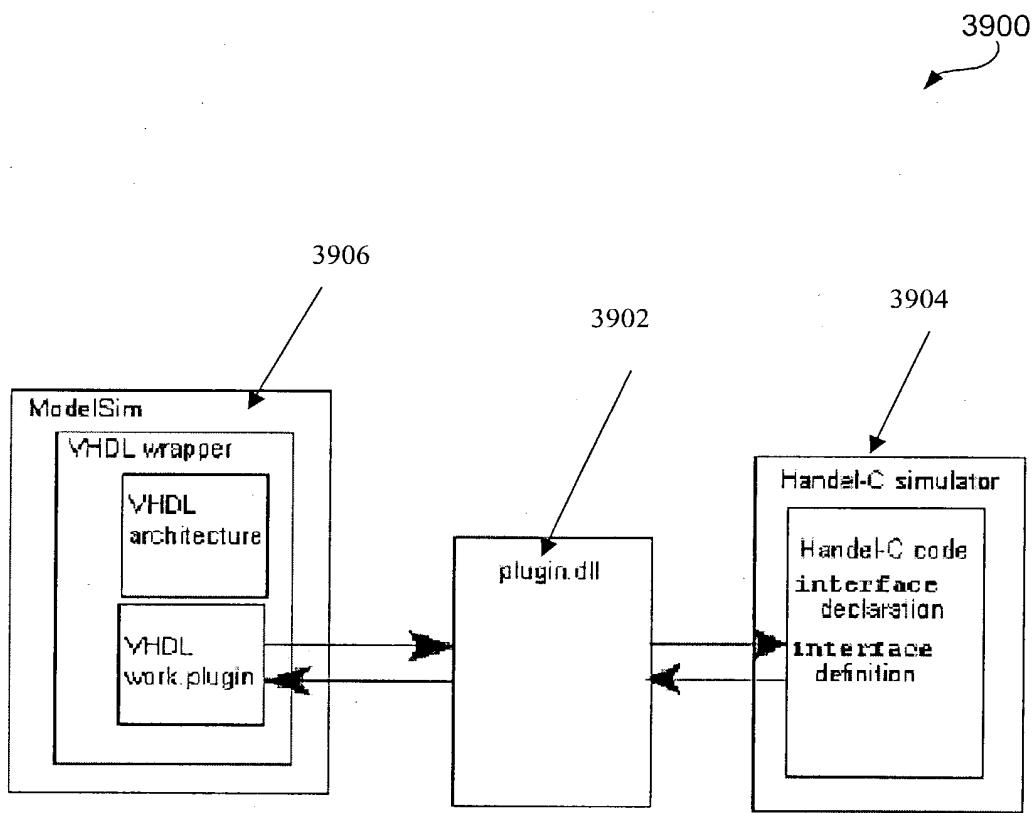
3702

**FIG. 37**

3800

interface port\_in(int 4 signals\_to\_HC with  
{busformat="B[1]}) read();  
would produce wires  
signals\_to\_HC[0]  
signals\_to\_HC[1]  
signals\_to\_HC[2]  
signals\_to\_HC[3]

**FIG. 38**



**FIG. 39**

Keyword	Function	Default
<b>base</b>	specify display base for variables in debugger	10
<b>extlib</b>	specify external plugin for simulator	None
<b>extfunc</b>	specify external simulator function for this port	PlugInSet or PlugInGet
<b>extpath</b>	specify any direct logic (combinatorial logic) connections to another port	None
<b>extinst</b>	specify connection to external code	None

**FIG. 40A**

4000

warn	disable some compiler warnings	No
------	--------------------------------	----

**FIG. 40B**

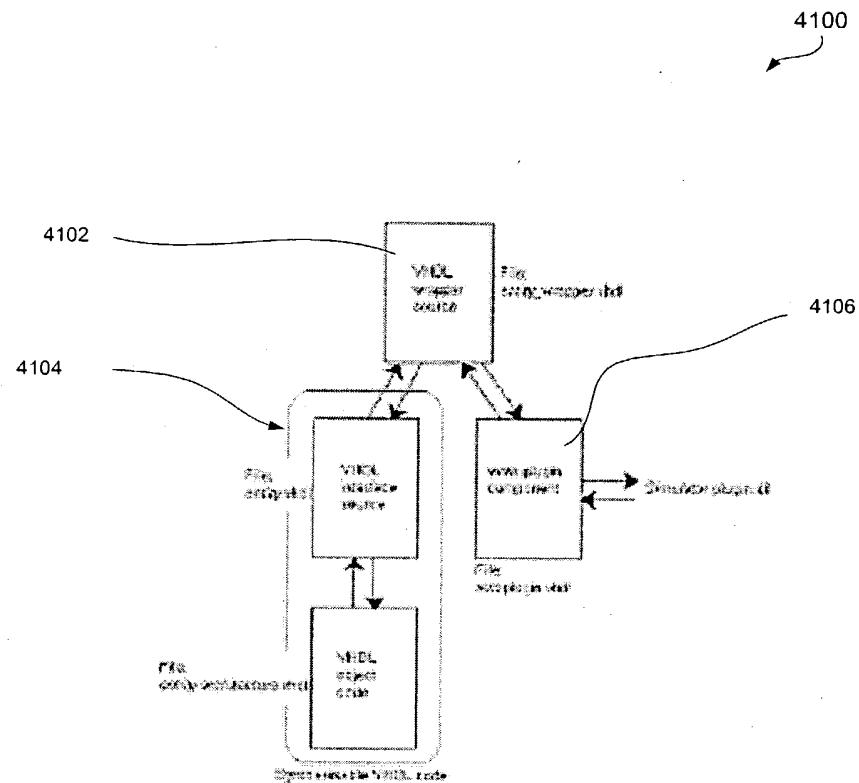


FIG. 41

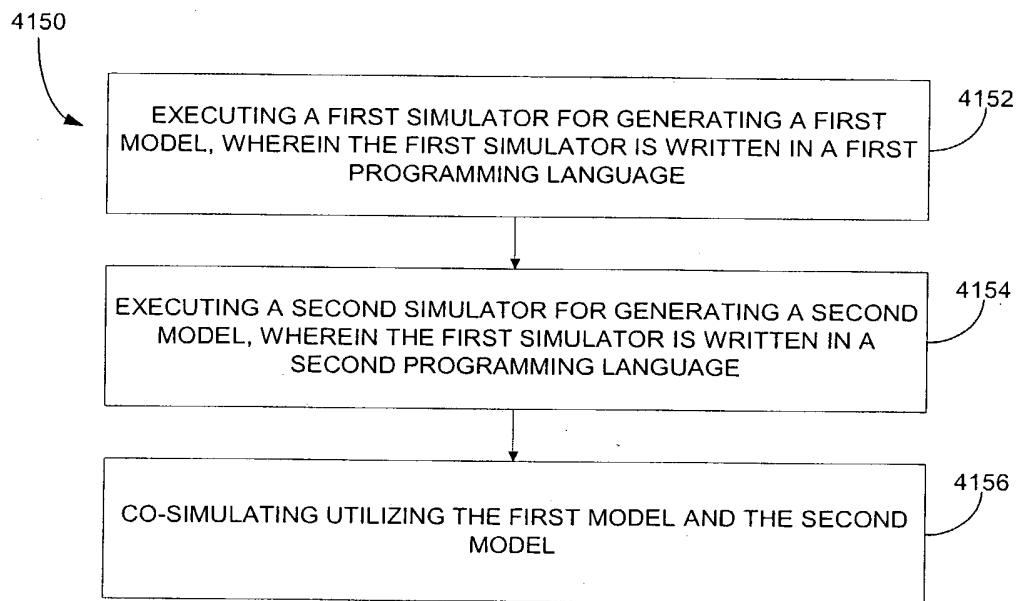


Fig. 41A

4200

When used	Function call	How often
First use of simulator in Handel-C session	PlugInOpen	once per plugin
Start of simulation	PlugInOpenPort	once per interface port using the plugin

**FIG. 42A**

4200

	<b>PluginOpenInstance</b>	once per instance (copy) of plugin
Simulator data transfer	<b>PluginSet</b>	called when data on a port sending data TO the plugin changes
	<b>PluginGet</b>	called whenever the simulator wishes to read data FROM the plugin
Start of simulated clock cycle	<b>PluginStartCycle</b>	
Middle of cycle	<b>PluginMiddleCycle</b>	called immediately before the simulator variables are updated
End of cycle	<b>PluginEndCycle</b>	
End of simulation	<b>PluginClosePort</b>	once per interface port using the plugin
	<b>PluginCloseInstance</b>	once per instance of the plugin
End of Handel-C session	<b>PluginClose</b>	once per plugin

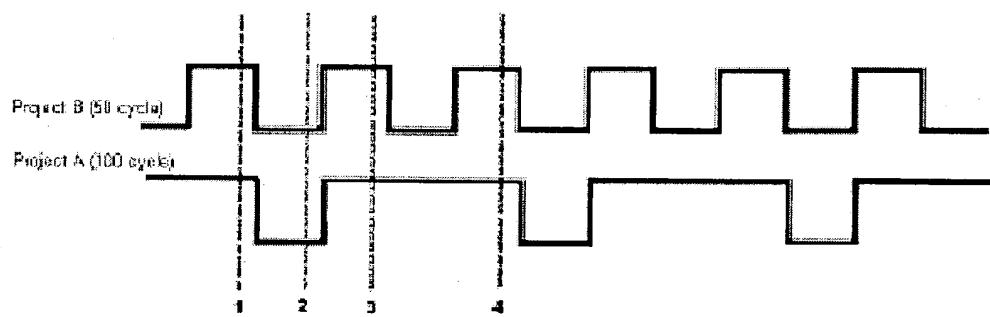
**FIG. 42B**

4300

	Possible Values	Default	Meaning
<b>ext lib</b>	Name of a plugin .dll	None	Specify external plugin for simulator
<b>ext func</b>	Name of a function within the plugin	PlugInSet or PlugInGet depending on port direction	Specify external function within the simulator for this port
<b>ext inst</b>	Instance name (with optional parameters)	None	Specify simulation instance used

**FIG. 43**

4400



**FIG. 44**

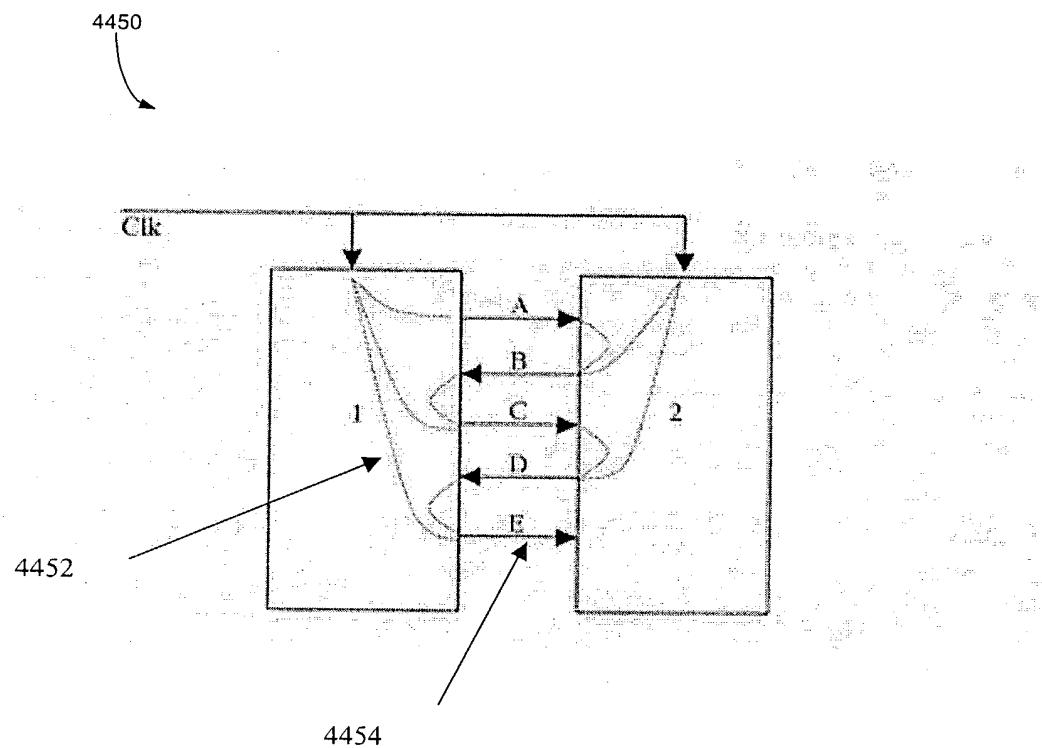


Fig. 44A

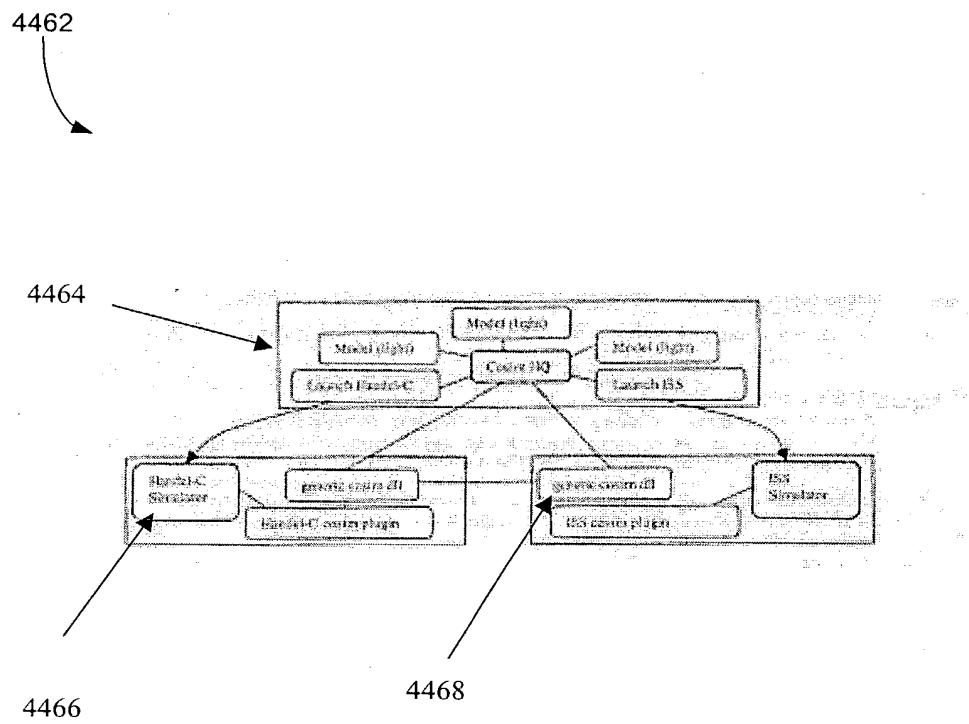


Fig. 44B

4470



4472

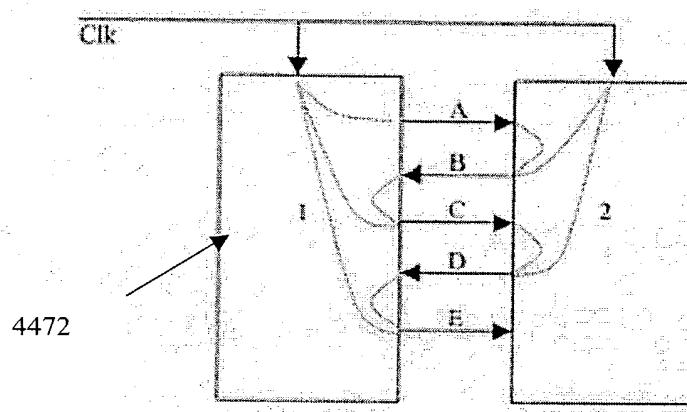
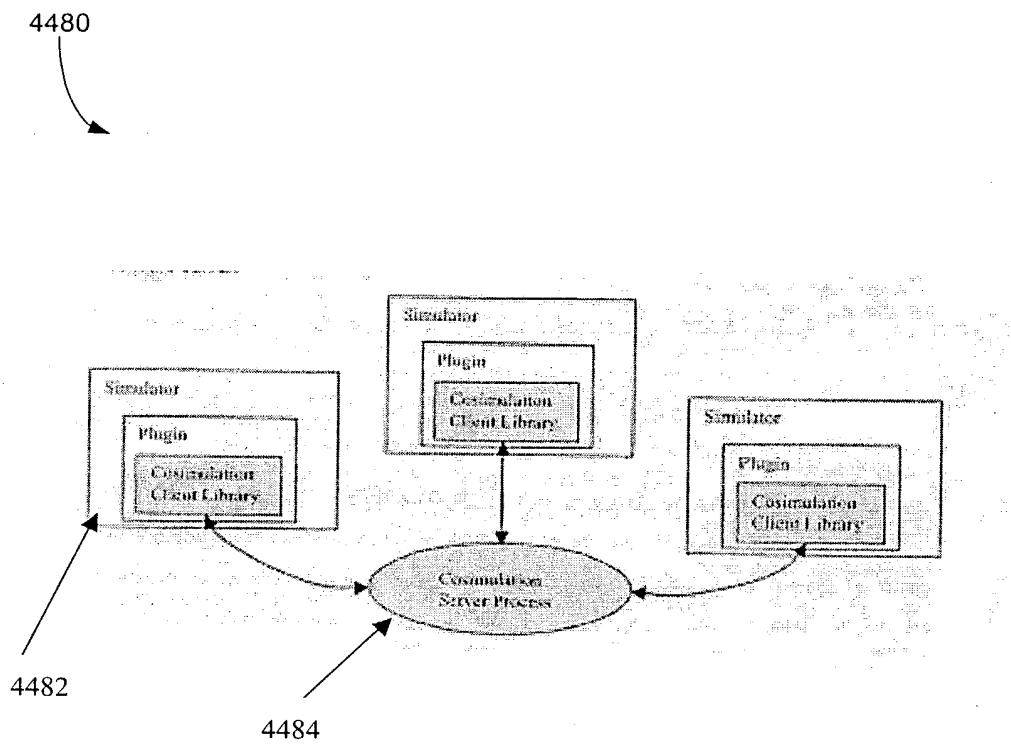


Fig. 44C



**Fig. 44D**

4500

Option	Meaning
<b>-c</b>	Compile only. Do not generate netlist. Output <code>.obj</code> file
<b>-s</b>	Target simulator
<b>-c1</b> <i>CommandLine</i>	Specify command line for compiling simulator output
<b>-f</b> <i>Family</i>	Specify target family
<b>-p</b> <i>Part</i>	Specify target part
<b>-edif</b>	Target EDIF output
<b>-vhdl</b>	Target VHDL output
<b>-lpm</b> <i>Width</i>	Use LPMs for data paths wider than <i>Width</i>
<b>-b</b>	Generate browse info database file
<b>-r</b> <i>filename</i>	Specify browse info database file name
<b>-o</b> <i>filename</i>	Specify output file name
<b>-xc</b> <i>filename</i>	Treat file as Handel-C source file
<b>-x1</b> <i>filename</i>	Treat file as Handel-C library file
<b>-xo</b> <i>filename</i>	Treat file as Handel-C object file
<b>-L</b> <i>Pathname</i>	Add <i>pathname</i> to library path
<b>-cpp</b> <i>Option</i>	Pass <i>Option</i> to preprocessor
<b>-D</b> <i>Symbol</i>	Define preprocessor symbol
<b>-E</b>	Preprocess source only
<b>-I</b> <i>Pathname</i>	Add <i>pathname</i> to preprocessor include path
<b>-U</b> <i>Symbol</i>	Undefine preprocessor symbol
<b>-O</b>	Turn on maximum optimisations
<b>-O-</b>	Turn off all optimisations
<b>-O+optimise</b>	Turn on <i>optimise</i> optimisation
<b>-O-optimise</b>	Turn off <i>optimise</i> optimisation
<b>Possible values for optimise</b>	
<b>cr</b>	Conditional rewriting optimisations

FIG. 45A

4500

	<b>cse</b>	CSE optimisations
	<b>high</b>	High-level optimisations.
	<b>pcse</b>	Partitioning CSE optimisations
	<b>rcse</b>	Repeated CSE optimisations.
	<b>rcr</b>	Repeated conditional rewriting optimisations.
	<b>retime</b>	Retiming optimisations.
	<b>rewrite</b>	Rewriting optimisations.
<b>-e</b>		Estimate logic depth and area. (Generate HTML files)
<b>-g</b>		Compile with debug information
<b>-W</b>		Show all warning messages
<b>-help</b>		Print help screen

**FIG. 45B**

4600

Command	Shortcut	Function
<b>Edit</b>		
<b>New...</b>	Ctrl+N	Display the <b>New</b> dialog
<b>Open.....</b>	Ctrl+O	Display the <b>File Open</b> dialog
<b>Save..</b>	Ctrl+S	Save the active document
<b>Print</b>	Ctrl+P	Print active document
<b>Undo</b>	Ctrl+Z	Reverse the most recent change to the active document or to the workspace
<b>Redo</b>	Ctrl+Y	Reverse the most recent undo
<b>Cut</b>	Ctrl+X	Copy the current selection and delete it
<b>Copy</b>	Ctrl+C	Copy the current selection to the clipboard
<b>Paste</b>	Ctrl+V	Copy the clipboard to the current selection
<b>Delete</b>	Del	Delete the current selection
<b>Breakpoints...</b>	Alt+F9	Display project's breakpoints dialog box
<b>View</b>		
<b>Workspace</b>	Alt+0	Hide or show the <b>Workspace</b> window
<b>Output</b>	Alt+2	Hide or show the <b>Output</b> window
<b>Debug Windows</b>		
<b>Watch</b>	Alt+3	Hide or show the <b>Watch</b> window
<b>Call Stack</b>	Alt+7	Hide or show the <b>Call Stack</b> window
<b>Memory</b>	Alt+6	Hide or show the <b>Memory</b> window
<b>Variables</b>	Alt+4	Hide or show the <b>Variables</b> window
<b>Clocks</b>	Alt+9	Hide or show the <b>Clocks</b> window
<b>Threads</b>	Alt+5	Hide or show the <b>Threads</b> window
<b>Properties</b>	Alt+Enter	Display properties of the current document or selection
<b>Project</b>		
<b>Settings...</b>	Alt+F7	Shows the <b>Project Settings</b> dialog box.
<b>Build</b>		
<b>Compile</b>	Ctrl+F7	Compile selected file.
<b>Build</b>	F7	Build this project

FIG. 46A

4600

Debug		
<b>Go</b>	F5	Run the simulator at full speed (until a breakpoint etc.)
<b>Restart</b>	Ctrl+Shift+F5	Run the simulator from the beginning.
<b>Stop Debugging</b>	Shift+F5	Stop the simulation
<b>Show Next Statement</b>	Alt + Num *	Run until the line containing the text cursor is reached.
<b>Step Into</b>	F11	Run to the first statement in the function invoked in the current line. If the current line is not a function invocation, just run until the next statement.
<b>Step Over</b>	F10	Run until the start of the next statement
<b>Step Out</b>	Shift+F11	Run until the start of the statement after the line which invoked the current function
<b>Run to Cursor</b>	Ctrl+F10	Run until the line containing the text cursor is reached.
<b>Advance</b>	Ctrl+F11	Run until the line containing the text cursor is reached.
Tools		
<b>Source Browser</b>	Alt+F12	Show a symbol browser dialogue box.
Help		
<b>Help Topics</b>	F1	List the Help topics
Output Window		
	Double click	Takes you to line in source code
	F4	Next error
	Shift + F4	Previous error
Windows control		
	F6	Next pane
	Shift + F6	Previous pane

FIG. 46B

4700

<b>Directory browsing</b>	
	Folder
	Network disc
	Removable disc
	RAM disc
	Folder (open)
	Fixed disc
	CDROM
<b>Output window</b>	
	Information
	User assert statement
	Error (in your program)
	Position stack
	Warning (about your program)
	Internal error in the compiler
	Position
<b>Source window</b>	
	Current active point
	Other statements executed in current thread on current clock cycle
	Active point in different thread
	Position of current error
	Breakpoint
	Disabled breakpoint
<b>Toolbar</b>	
	New Text File
	New ...
	Open
	Save
	Save All
	Print
	Cut
	Copy
	Paste
	Undo
	Redo
	Show Workspace window
	Show Output window
	Show properties
	Compile one file
	Build project
	Stop a build in progress
	Run program in simulator
	Add or remove breakpoint
	Show about box

**FIG. 47A**

4700

**Debug**

-  Restart,
-  Stop debugging
-  Step in
-  Step out,
-  Run to cursor
-  Show watch windows
-  Show call stack window
-  Clock in clocks window
-  Thread in threads window
-  Pause
-  Step over,
-  Advance

**Workspace window**

**File view**

-  Handel-C workspace (.hw file)
-  Handel-C system project (.hp file)
-  Handel-C board project (.hp file)
-  Handel-C chip project (.hp file)
-  Handel-C core project (.hp file)
-  Library project (.hp file)
-  Document (.txt, .h)
-  Source file (.c file)
-  Folder
-  Folder (open)

**FIG. 47B**

4700

#### Symbol view

- ⌚ Target (used for configurations)
- ☰ Function or shared proc or expr
- ⌚ In-line function, macro
- ⌚ Variable
- ⌚ RAM, ROM or WOM variable
- ⌚ Channel (chan, chanin or chanout)
- ⌚ Signal
- ⌚ Interface
- ⌚ Position stack
- ⌚ Position

#### Browsing

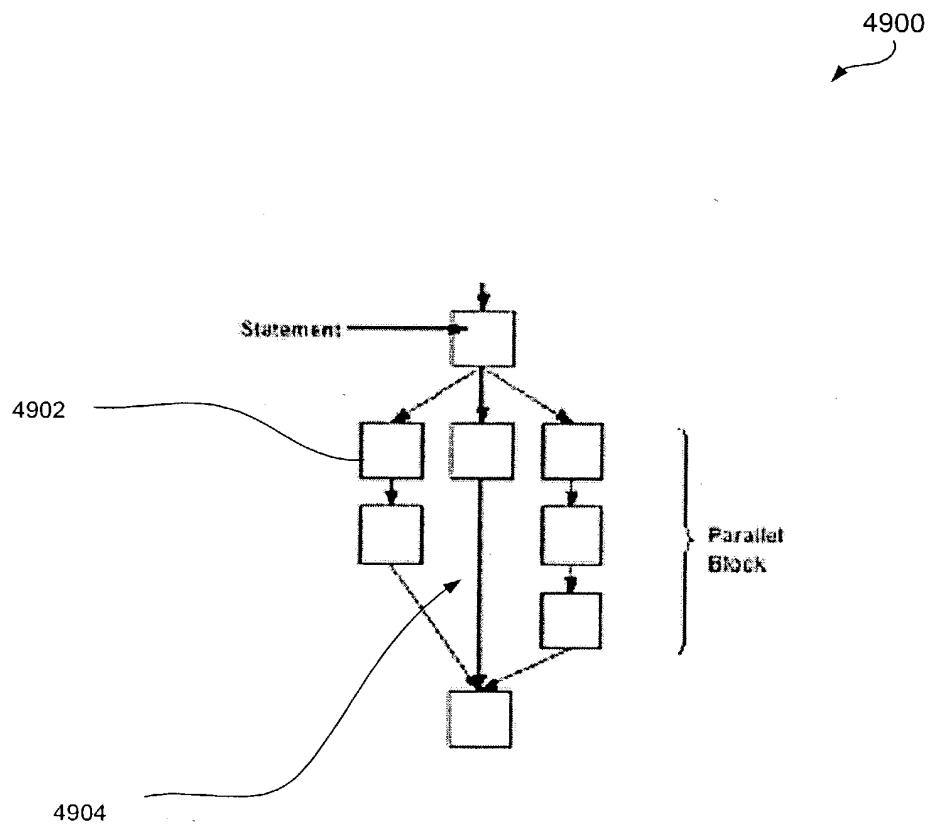
- ⌚ Go to definition
- ⌚ Go to reference
- ⌚ Previous
- ⌚ Next
- ⌚ Return to original context
- ⌚ File outline
- ⌚ Definitions and references

**FIG. 47C**

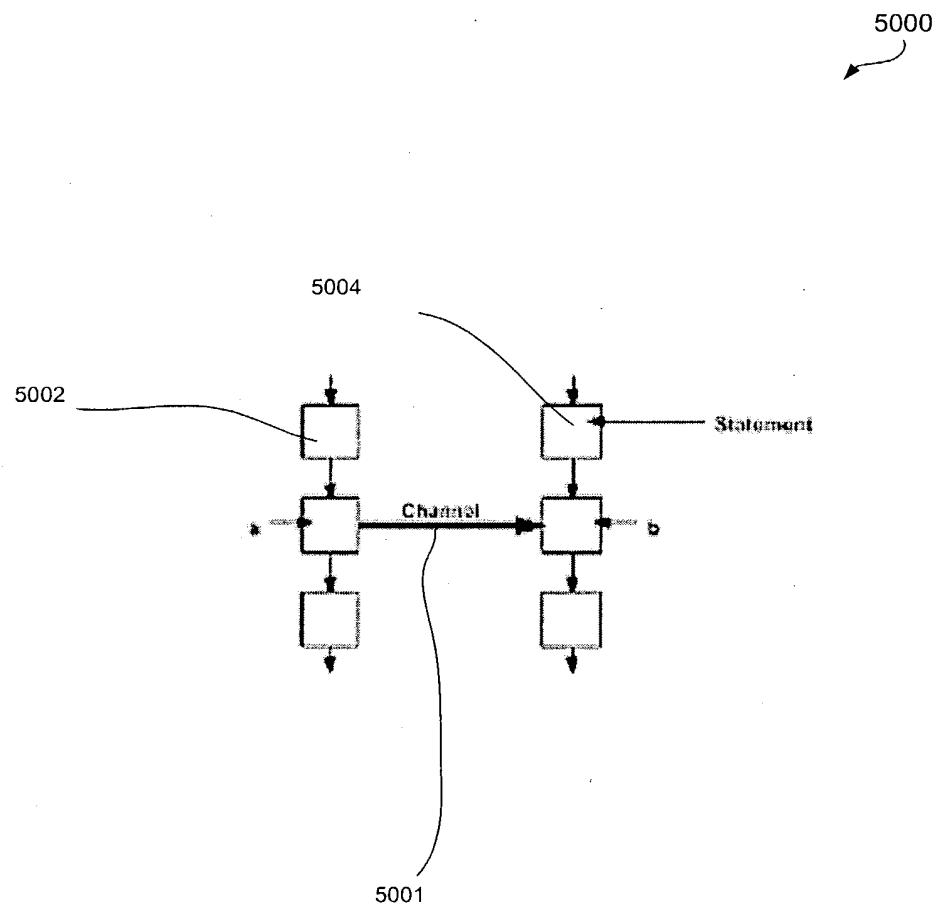
4800

Raw file bit number	Colour bit
7 (Most significant)	Red 7
6	Green 7
5	Blue 7
4	Blue 6
3	Green 6
2	Red 6
1	Green 5
0 (Least significant)	Green 4

**FIG. 48**

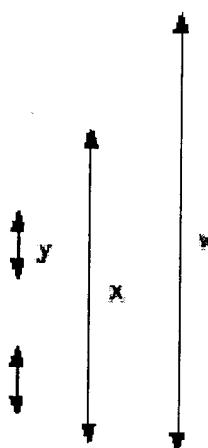


**FIG. 49**



**FIG. 50**

int w;  
void main(void)  
{  
 int x;  
 {  
 int y;  
 ....  
 }  
 int z;  
 ....  
}



5100

**FIG. 51**

Operator	Meaning	ISO-C	Change in Version 3
[]	array index delimiters, bit selection	Extended	Array index may be a variable, bit selection may not
*	structure, union and multi-port RAM member operator, interface port operator	Yes	struct variables have been added
*	indirection operator	Yes	New
&	address operator	Yes	New
/	division operator	Yes	Extended: division of variables
%	modulus operator	Yes	Extended: modulus of variables
<<	left-shift operator	Yes	Extended: shift by variable amounts
>>	right shift operator	Yes	Extended: shift by variable amounts

FIG. 52

## Declarations

Keyword	Meaning	ISO-C	Change in v.3
<code>&lt;&gt;</code>	<b>disambiguator</b>	No	New
<code>auto</code>	auto variable	Yes	New
<code>const</code>	specify that variable's value will not change	Yes	New
<code>enum</code>	enumeration constant	Yes	New
<code>extern</code>	define global variable	Yes	New
<code>inline</code>	<b>declaration of inline function</b>	No	New
<code>interface</code>	<b>declaration of off-chip interface</b>	No	Extended: you can now create interfaces to foreign code
<code>mpram</code>	<b>declare a multi-port RAM</b>	No	Create dual-ported RAMs
<code>ram</code>	<b>declare a RAM</b>	No	Extended to specify Xilinx block memory
<code>register</code>	declare register variable	Yes	New
<code>rom</code>	<b>declare a ROM</b>	No	Extended to specify Xilinx block memory
<code>signal</code>	<b>declare a signal object</b>	No	New
<code>signed</code>	declare a signed variable	Yes	New
<code>static</code>	specify variable with limited scope	Yes	New
<code>struct</code>	declare a structure variable	Yes	New
<code>typedef</code>	define type	Yes	New
<code>void</code>	specify void return type or empty parameter list	Yes	New
<code>volatile</code>	declare volatile variable	Yes	New
<code>wom</code>	<b>declare a WOM (array)</b>	No	Specify an area of write-only memory

FIG. 53

**Statements**

Statement	Meaning	ISO-C	Change in v.3
assert	diagnostic macro to print to stderr	Not standard	Print string to standard error channel
continue	continue execution outside code block	Yes	New
goto	jump to specified label	Yes	New
ifselect	conditional execution on compile time selection	No	Compile following code if selected, else...
par	execute statements in parallel	No	Extended: parallel statements can be replicated
return	return from function	Yes	New
seq	execute statements in sequence	No	New: seq blocks can also be replicated
typeof	return type of operator	No	As in GNU C

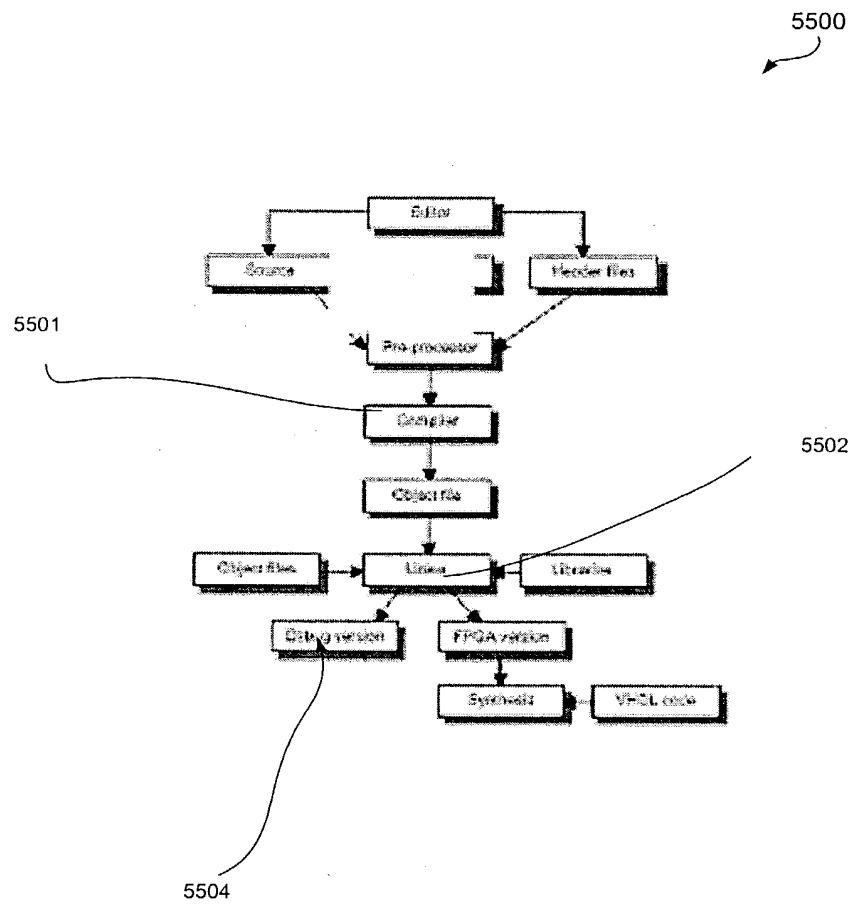
**Macros**

Keyword	Meaning	ISO-C	Change in version 3
in	define scope for local macro expression declaration	No	New: let macro expr name = expression in macro expression
let	start declaration of local macro expression	No	New: let macro expr name = expression in macro expression

**Clocks**

Keyword	Meaning	ISO-C	Change in version 3
internal	use internal clock	No	Extended: can use any expression
Internal_divide	use divided internal clock	No	Extended: can use any expression
_clock	use current clock	No	New

**FIG. 54**



**FIG. 55**

5600

Predefined bus interface specs:		Default
<b>data</b>	list the pins used for transferring data, MSB to LSB	None
<b>speed</b>	set buffer speed (output)	Xilinx = 3 Altera = 1
<b>pull</b>	set pull-up or pull-down for bus pins (not Altera)	None
<b>infile</b>	set file source for input bus data	None
<b>outfile</b>	set file destination for output bus data	None

All interface specs		Default
<b>base</b>	specify display base for variables in debugger	10
<b>extlib</b>	specify external plugin for simulator	None
<b>extfunc</b>	specify external simulator function for this port	PlugInSet or PlugInGet
<b>extpath</b>	specify any direct logic (combinatorial logic) connections to another port	None
<b>extinst</b>	specify connection to external code	None
<b>warn</b>	disable some compiler warnings	No

**FIG. 56**

5700

ROM entry	Value	ROM entry	Value
$b[0][0][0]$	1	$b[0][0][1]$	2
$b[0][1][0]$	3	$b[0][1][1]$	4
$b[1][0][0]$	5	$b[1][0][1]$	6
$b[1][1][0]$	7	$b[1][1][1]$	8
$b[2][0][0]$	9	$b[2][0][1]$	10
$b[2][1][0]$	11	$b[2][1][1]$	12
$b[3][0][0]$	13	$b[3][0][1]$	14
$b[3][1][0]$	15	$b[3][1][1]$	16

FIG. 57

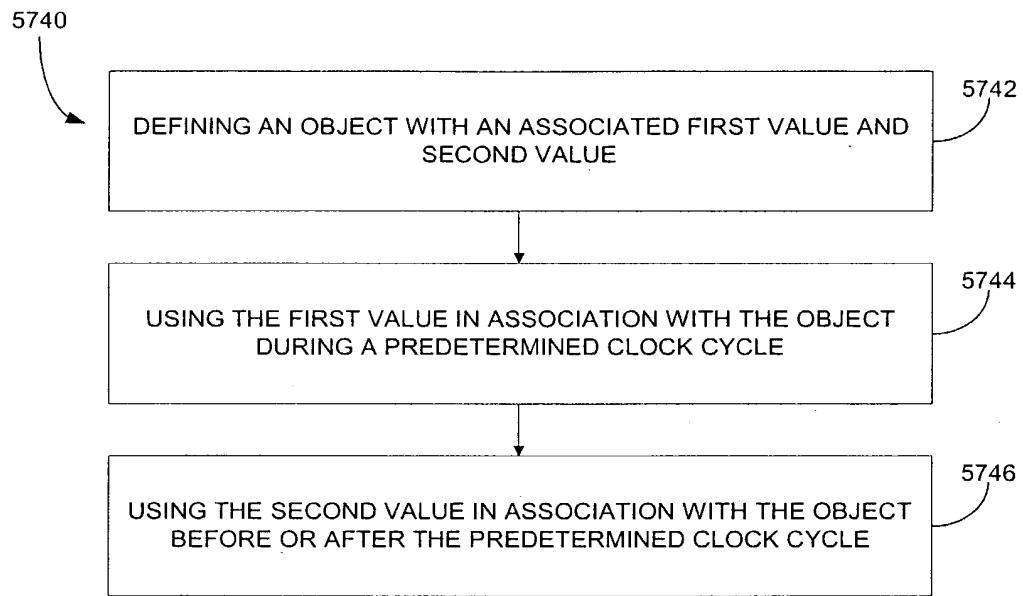


Fig. 57A

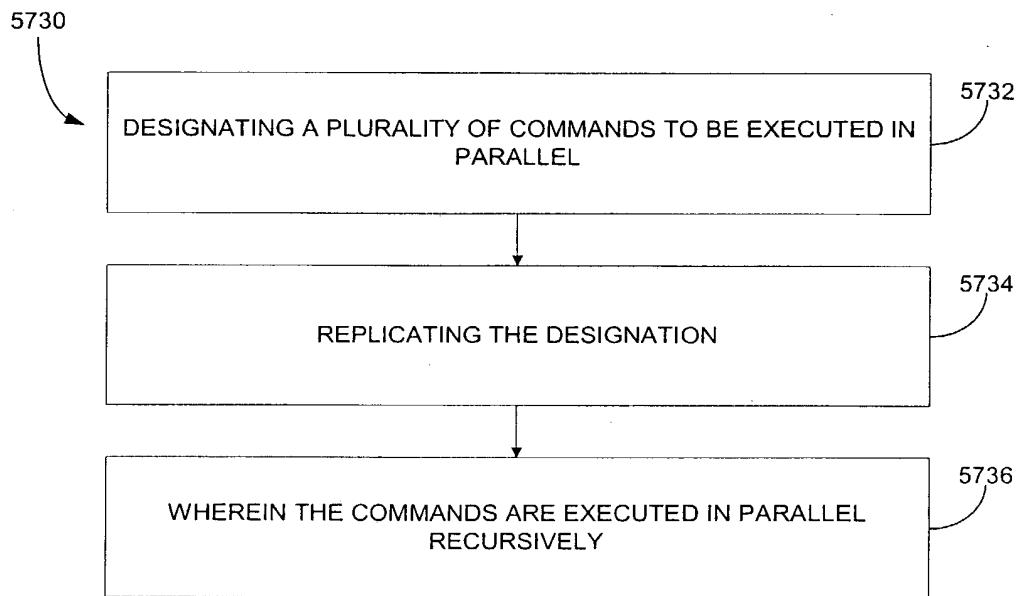


Fig. 57A-1

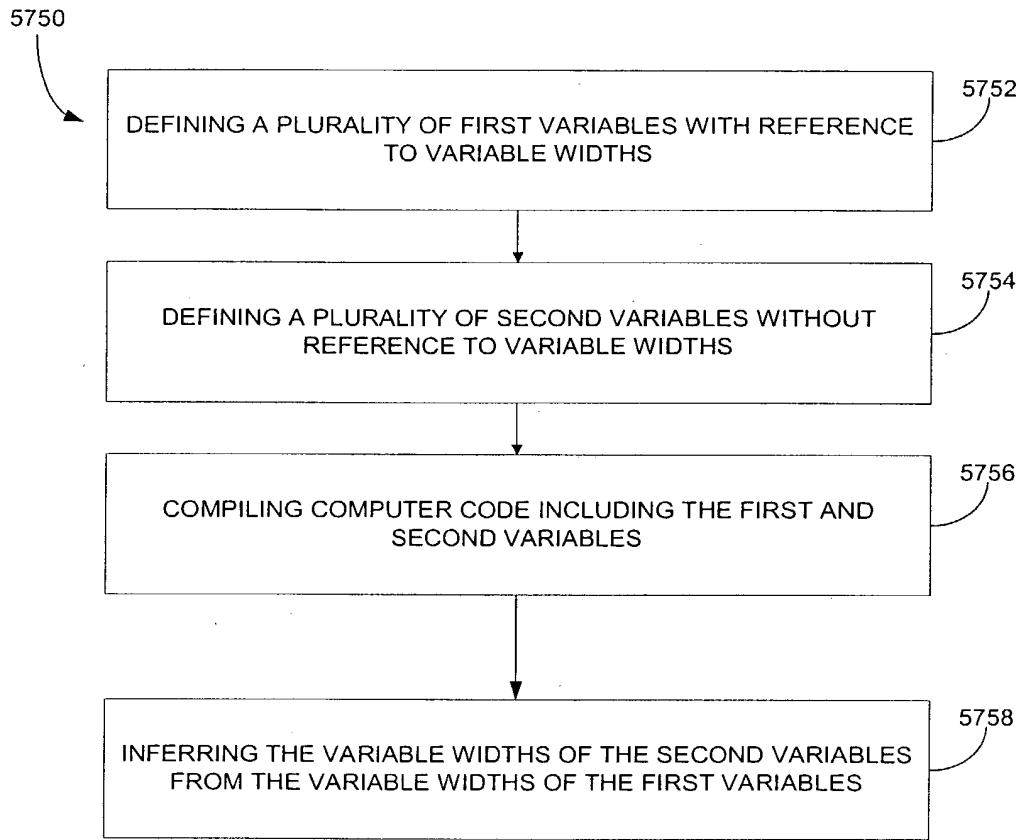


Fig. 57A-2

Statement	Timing
{...}	Sum of all statements in sequential block
par {...}	Length of longest branch in block
Function(), break, goto, continue	No clock cycles
return(Expression);	1 clock cycle if Expression is assigned on return, otherwise none.
Variable = Expression;	1 clock cycle
Variable ++;	1 clock cycle
Variable --;	1 clock cycle
++ Variable;	1 clock cycle
-- Variable;	1 clock cycle
Variable += Expression;	1 clock cycle
Variable -= Expression;	1 clock cycle
Variable *= Expression;	1 clock cycle
Variable /= Expression;	1 clock cycle
Variable %= Expression;	1 clock cycle
Variable <= Constant;	1 clock cycle
Variable >= Constant;	1 clock cycle
Variable &= Expression;	1 clock cycle
Variable  = Expression;	1 clock cycle
Variable ^= Expression;	1 clock cycle
Channel ? Variable;	1 clock cycle when transmitter is ready (in same clock domain)

FIG. 58A

Statement	Timing
Channel I Expression;	1 clock cycle when receiver is ready (in same clock domain)
if (Expression) {...} else {...}	Length of executed branch
while (Expression) {...}	Length of loop body * number of iterations
do {...} while (Expression);	Length of loop body * number of iterations
for (Init; Test; Iter) {...}	Length of Init + (Length of body + length of Iter) * number of iterations
switch (Expression) {...}	Length of executed case branch
prialt {...}	1 clock cycle for case communication when other party is ready plus length of executed case branch or length of default branch if present and no communication case is ready or infinite if no default branch and no communication case is ready
delay;	1 clock cycle

FIG. 58B

5900

Clock	in	x[0]	x[1]	x[2]	out
1	5	0	0	0	0
2	6	5	0	0	0
3	7	6	5	0	0
4	8	7	6	5	0
5	9	8	7	6	5
6	10	9	8	7	6
7	11	10	9	8	7
8	12	11	10	9	8
	13	12	11	10	9

FIG. 59

6000

Location	Meaning
<b>internal Frequency</b>	Clock from internal clock generator (Xilinx 4000 series devices only).
<b>internal Expression</b>	
<b>internal_divide Frequency Factor</b>	Clock from internal clock generator with integer division (Xilinx 4000 series devices only).
<b>internal_divide Expression</b>	
<b>external [Pin]</b>	Clock from device pin.
<b>external_divide [Pin] Factor</b>	Clock from device pin with integer division.

**FIG. 60**

6100

Family Name	Description
Xilinx4000E	4000E series Xilinx FPGAs
Xilinx4000L	4000L series Xilinx FPGAs
Xilinx4000EX	4000EX series Xilinx FPGAs
Xilinx4000XL	4000XL series Xilinx FPGAs
Xilinx4000XV	4000XV series Xilinx FPGAs
XilinxVirtex	Virtex Xilinx FPGAs
Altera10K	Flex10K series Altera FPGAs
Altera20K	Flex20K series Altera FPGAs

**FIG. 61**

6200

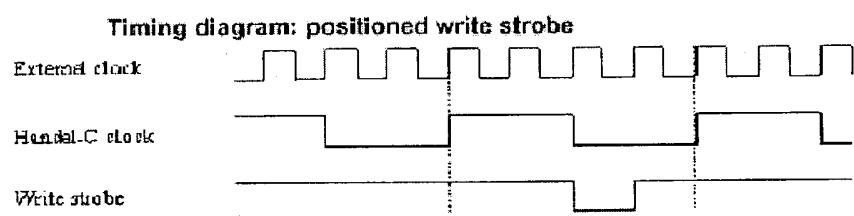


FIG. 62

6300

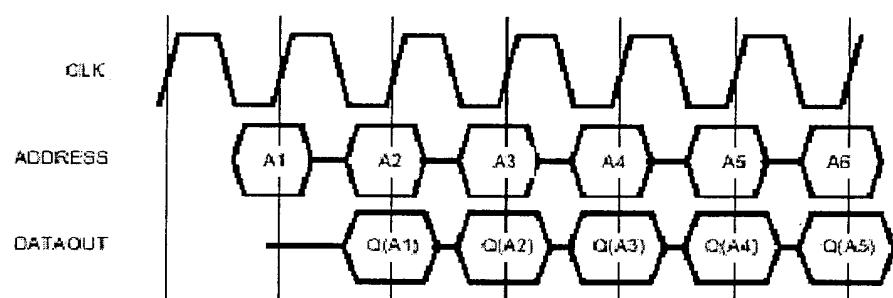


FIG. 63

6400

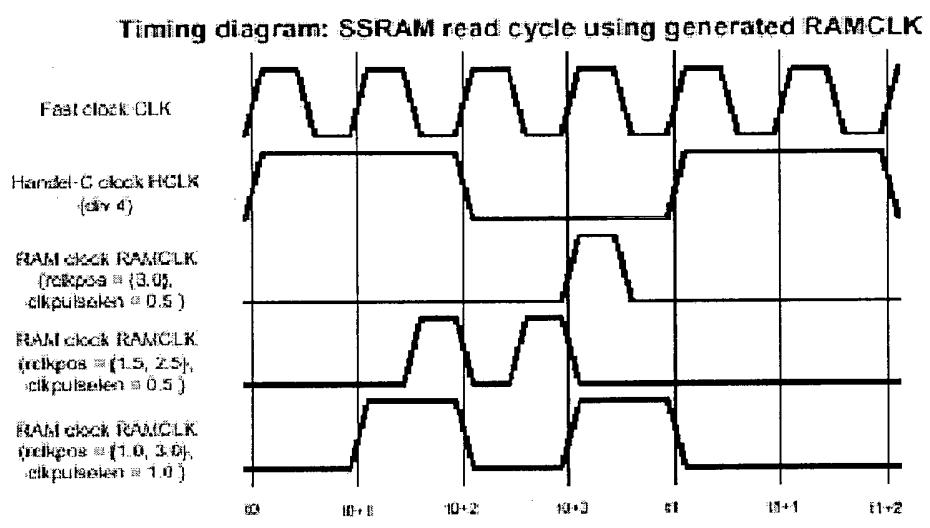


FIG. 64

6500

Read-cycle from a flow-through SSRAM within a Handel-C design.

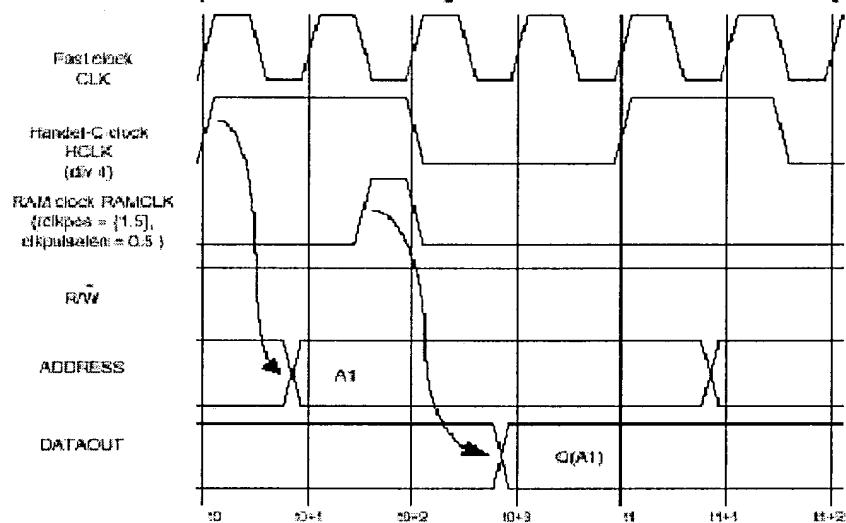


FIG. 65

6600

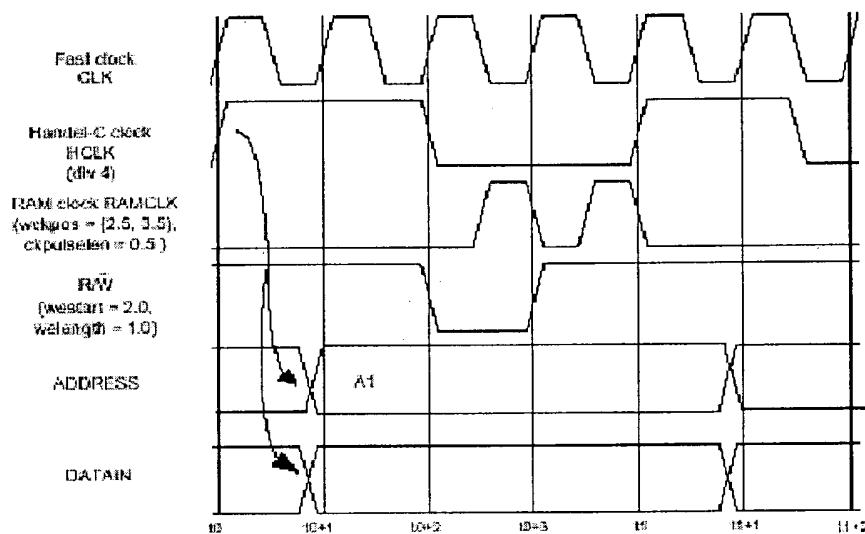


FIG. 66

6700

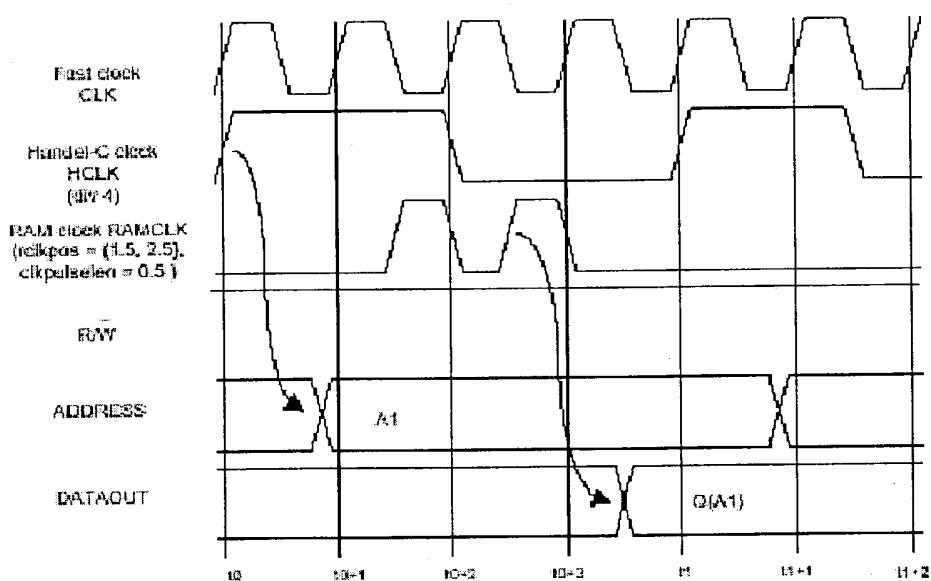
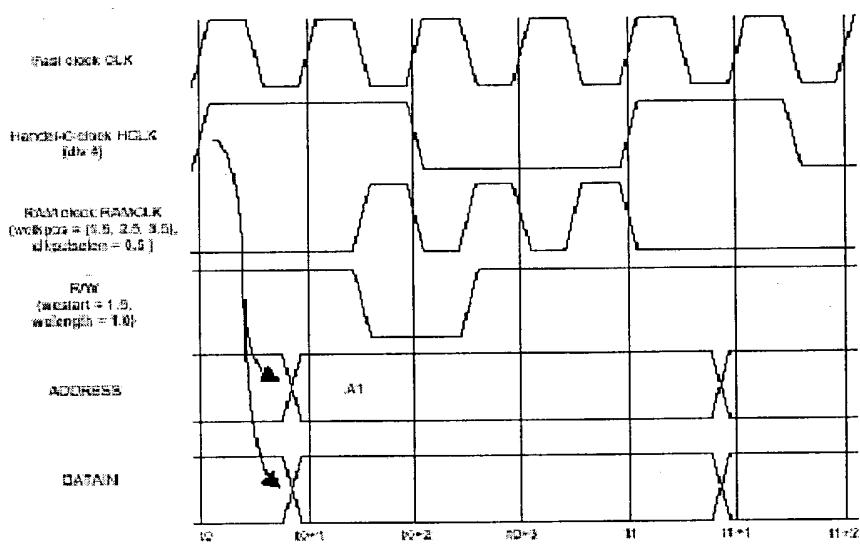


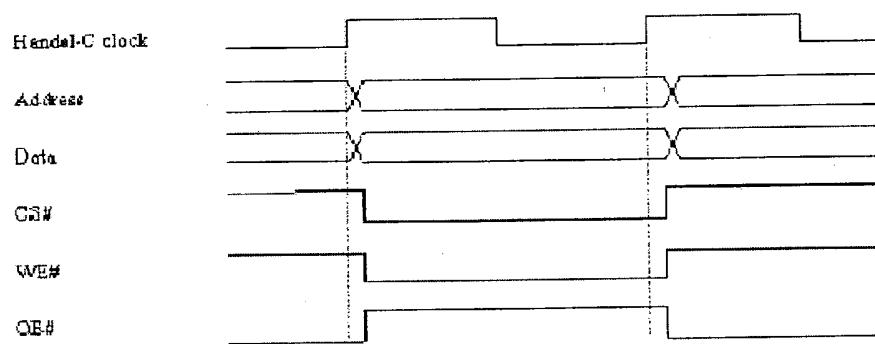
FIG. 67

6800



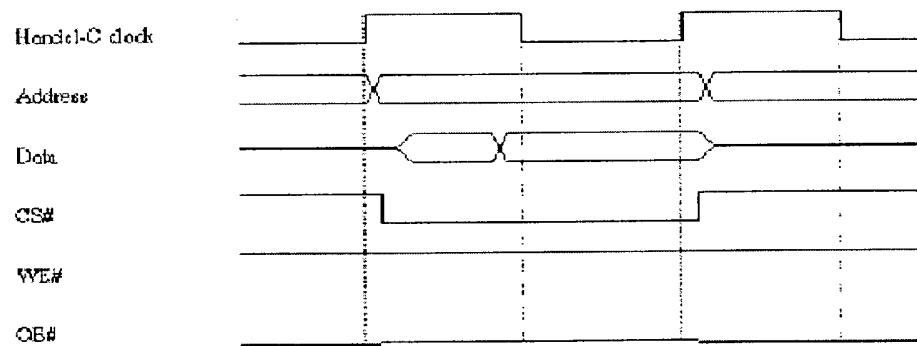
**FIG. 68**

6900



**FIG. 69**

7000



**FIG. 70**

7100

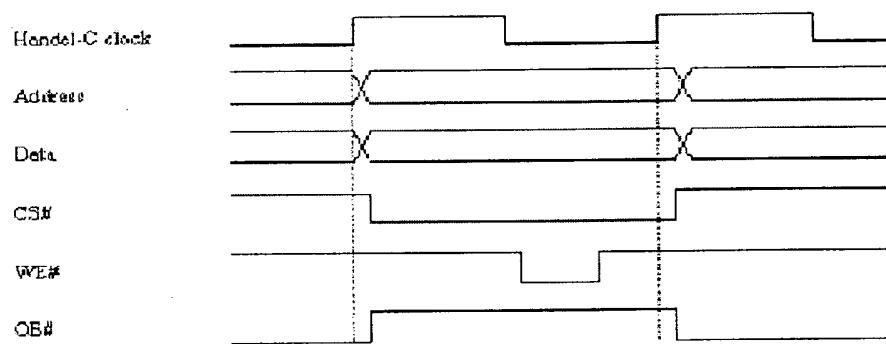
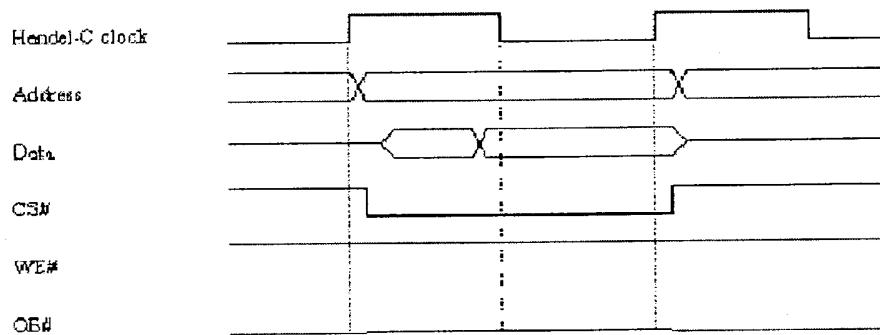


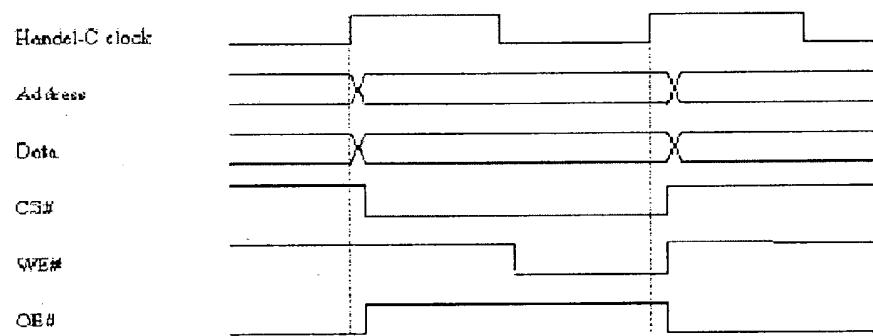
FIG. 71

7200



**FIG. 72**

7300



**FIG. 73**

7400

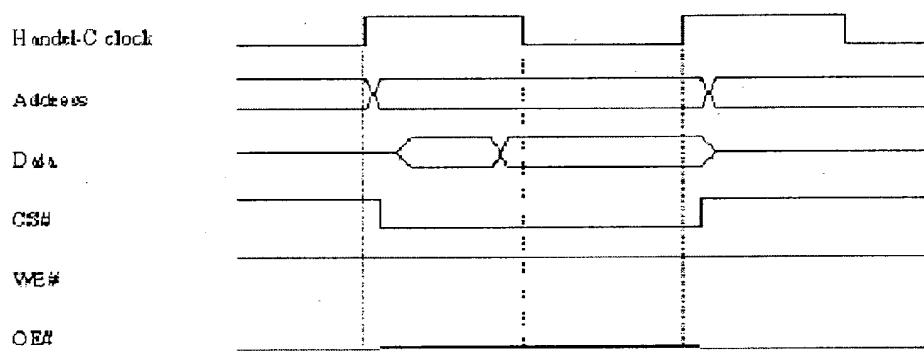


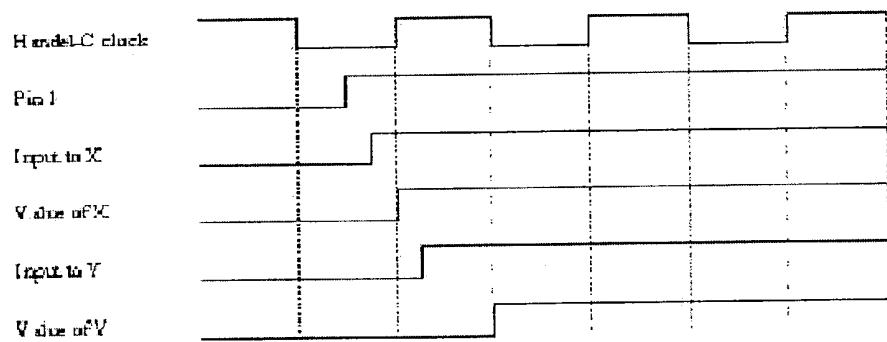
FIG. 74

7500

Sort Identifier	Description
bus_in	Input bus from pins
bus_latch_in	Registered input bus from pins
bus_clock_in	Clocked input bus from pins
bus_out	Output bus to pins
bus_ts	Bi-directional tri-state bus
bus_ts_latch_in	Bi-directional tri-state bus with registered input
bus_ts_clock_in	Bi-directional tri-state bus with clocked input
port_in	Input port from logic
port_out	Output port to logic

FIG. 75

7600



**FIG. 76**

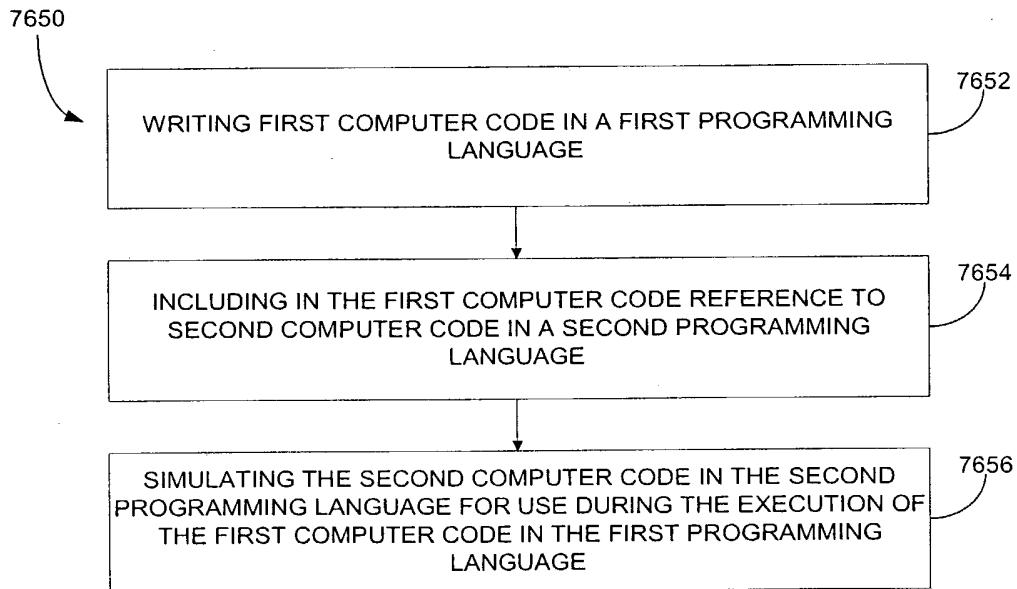
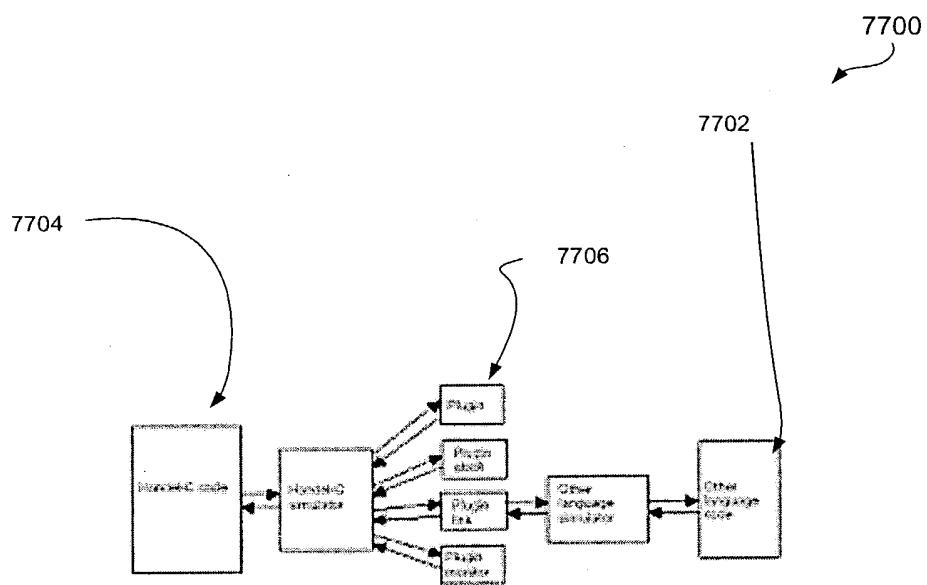


Fig. 76A



**FIG. 77**

7800

Specification	Possible Values	Default	Applies to	Meaning
show	0, 1	1	variables channels o/p buses tri-state buses	Show variable during simulation
base	2, 8, 10, 16	10	variables o/p channels o/p buses tri-state buses	Print variable in specified base
infile	Any valid filename	None	chanins i/p buses tri-state buses	Redirect from file
outfile	Any valid filename	None	chanouts o/p buses tri-state buses	Redirect to file
warn	0, 1	1	variables memories channels buses	Enable warnings for object
speed	0, 1, 2, 3 Xilinx = 3 Altera = 1	Xilinx = 3 Altera = 1	o/p or tri-state bus	Set buffer speed
intime	Any floating point ns delay	None	input port or bus or tri-state bus external RAMs	Maximum allowable delay between interface and variable
outtime	Any floating point ns delay	None	output port or bus or tri-state bus external RAMs	Maximum allowable delay between variable and interface
extlib	Name of a plugin .d11	None	interface or port	Specify external plugin for simulator

FIG. 78A

Specification	Possible Values	Default	Applies to	Meaning
<b>extfunc</b>	Name of a function within the plugin	PluginSet or PluginGet depending on port direction	interface or port	Specify external function within the simulator for this port
<b>extpath</b>	Name of port TO Handel-C on the same interface	None	port FROM Handel-C	Specify any direct logic (combinatorial logic) connections to another port
<b>extinst</b>	Instance name (with optional parameters)	None	interface or port	Specify simulation instance used
<b>busformat</b>	Format string	B_1	interface, port or memories in external logic	Specify the way that wire names are formatted in EDIF
<b>pull</b>	0, 1	None	Xilinx buses	Add pull up or pull down resistor(s)
<b>data</b>	Any valid pin list	None	memories buses	Set data pins
<b>offchip</b>	0, 1	0	memories	Set RAM/ROM to be off chip
<b>ports</b>	0, 1	0	memories	Set RAM/ROM to be in external code
<b>block</b>	0, 1	Xilinx=0 Altera=1	memories (on-chip)	Set RAM/ROM to be in block memory
<b>wegate</b>	-1, 0, 1	0	RAMs	Place write enable signal
<b>westart</b>	0 to clock division -1	None	RAMs	Position write enable signal
<b>welength</b>	1 to clock division	None	RAMs	Set length of write enable signal
<b>rclkpos</b>	Any number of cycles or half-cycles	None	SSRAM	Set read cycle position of SSRAM clock
<b>wclkpos</b>	Any number	None	SSRAM	Set write cycle position of SSRAM clock

FIG. 78B

7800

Specification	Possible Values	Default	Applies to	Meaning
	of cycles or half-cycles			position of SSRAM clock
clkpulseten	Any number of cycles or half-cycles	None	SSRAM	Set pulse length of SSRAM clock
clk	Any valid pin list	None	SSRAM (off-chip)	Set clock pins for external SSRAM clock
addr	Any valid pin list	None	memories (off-chip)	Set address pins
oe	Any valid pin list	None	memories (off-chip)	Set output enable pin(s)
we	Any valid pin list	None	RAMs (off-chip)	Set write enable pin(s)
cs	Any valid pin list	None	memories (off-chip)	Set chip select pin(s)
rate	Any floating point ns delay	None	clock	Maximum allowable inter-component delay

FIG. 78C

7850

Specification	Input bus	Output bus	Tri-state bus	RAM	ROM
addr				✓	✓
data	✓	✓	✓	✓	✓
we				✓	
cs				✓	✓
oe				✓	✓
clk				✓	

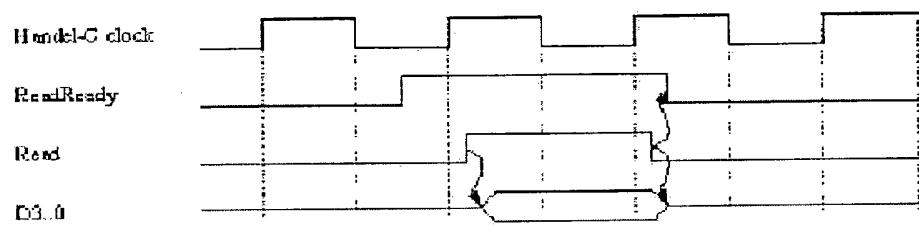
FIG. 78D

7900

Signal Name	FPGA pin	Description
D3..0	1, 2, 3, 4	Data Bus
Write	5	Write strobe
Read	6	Read strobe
WriteRdy	7	Able to write to device
ReadRdy	8	Able to read from device

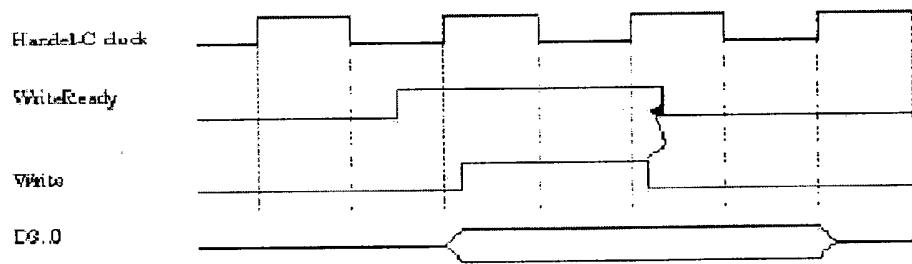
**FIG. 79**

8000



**FIG. 80**

8100



**FIG. 81**

8200

Type	Width
[signed   unsigned] char	8 bits
[signed   unsigned] short	16 bits
[signed   unsigned] long	32 bits
[signed   unsigned] int	See note 1
[signed   unsigned] int n	n bits
[signed   unsigned] int undefined	Compiler infers width
typeof (Expression)	Yields type of object

Note 1: Width will be inferred by compiler unless the 'set intwidth = n' command appears before the declaration

**FIG. 82**

8300

Prefix	Object
chan	Channel
chanin	Simulator channel
chanout	Simulator channel
ram	Internal or external RAM
rom	Internal or external ROM
signal	Wire
wom	WOM within multi-port memory

The compound types are:

Prefix	Object
struct	Structure
mpram	Multi-port memory

**FIG. 83**

Statement	Meaning
<code>par { ... }</code>	Parallel composition
<code>seq { ... }</code>	Sequential execution
<code>par (Init ; Test ; Iter) { ... }</code>	Parallel replication
<code>seq (Init ; Test ; Iter) { ... }</code>	Sequential replication
<code>Variable = Expression;</code>	Assignment
<code>Variable ++;</code>	Increment
<code>Variable --;</code>	Decrement
<code>++ Variable;</code>	Increment
<code>-- Variable;</code>	Decrement
<code>Variable += Expression;</code>	Add and assign
<code>Variable -= Expression;</code>	Subtract and assign
<code>Variable *= Expression;</code>	Multiply and assign
<code>Variable /= Expression;</code>	Divide and assign
<code>Variable %= Expression;</code>	Modulus and assign
<code>Variable &lt;= Expression;</code>	Shift left and assign
<code>Variable &gt;= Expression;</code>	Shift right and assign
<code>Variable &amp;= Expression;</code>	AND and assign
<code>Variable  = Expression;</code>	OR and assign
<code>Variable ^= Expression;</code>	XOR and assign
<code>Channel ? Variable;</code>	Channel input
<code>Channel ! Expression;</code>	Channel output
<code>if (Expression) { ... } else { ... }</code>	Conditional execution
<code>ifselect (Expression) { ... } else { ... }</code>	Conditional compilation
<code>while (Expression) { ... }</code>	Iteration
<code>do { ... } while (Expression);</code>	Iteration
<code>for (Init ; Test ; Iter) { ... }</code>	Iteration
<code>break;</code>	Loop and switch termination
<code>continue;</code>	Resume execution
<code>return[[Expression]];</code>	Return from function
<code>goto label;</code>	Jump to label
<code>switch (Expression) { ... }</code>	Selection
<code>prialt { ... }</code>	Channel alternation
<code>delay;</code>	Single cycle delay

Note: RAM and ROM elements, signals and array elements are included in the set of variables in this table.

**FIG. 84**

Operator	Meaning
<code>select(Constant, Expr, Expr)</code>	Compile-time selection
<code>Expression [Expression]</code>	Array or memory subscripting
<code>Expression [Constant]</code>	Bit selection
<code>Expression [Constant: Constant]</code>	Bit range extraction. One of the two constants may be omitted
<code>functionName (Arguments)</code>	Function call <sup>1</sup>
<code>pointerToStructure-&gt;member</code>	Structure reference
<code>structureName.member</code>	Structure reference
<code>! Expression</code>	Logical NOT
<code>~ Expression</code>	Bitwise NOT
<code>- Expression</code>	Unary minus
<code>+ Expression</code>	Unary plus
<code>&amp; object</code>	Yields pointer to operand
<code>* pointer</code>	Yields object or function that the operand points to
<code>(Type) Expression</code>	Type casting
<code>width(Expression)</code>	Width of expression
<code>Expression &lt;- Constant</code>	Take LSBs
<code>Expression \\&lt; Constant</code>	Drop LSBs
<code>Expression * Expression</code>	Multiplication
<code>Expression / Expression</code>	Division
<code>Expression % Expression</code>	Modulus arithmetic
<code>Expression + Expression</code>	Addition
<code>Expression - Expression</code>	Subtraction
<code>Expression &lt;&lt; Expression</code>	Shift left
<code>Expression &gt;&gt; Expression</code>	Shift right
<code>Expression @ Expression</code>	Concatenation
<code>Expression &lt; Expression</code>	Less than
<code>Expression &gt; Expression</code>	Greater than

FIG. 85A

8500

Operator	Meaning
<i>Expression &lt;= Expression</i>	Less than or equal
<i>Expression &gt;= Expression</i>	Greater than or equal
<i>Expression == Expression</i>	Equal
<i>Expression != Expression</i>	Not equal
<i>Expression &amp; Expression</i>	Bitwise AND
<i>Expression ^ Expression</i>	Bitwise XOR
<i>Expression   Expression</i>	Bitwise OR
<i>Expression &amp;&amp; Expression</i>	Logical AND
<i>Expression    Expression</i>	Logical OR
<i>Expression ? Expr : Expr</i>	Conditional selection

FIG. 85B

Keyword	Meaning	ISO-C	New in version 3
=	assignment operator	Yes	
;	statement terminator	Yes	
,	C only	Yes	
{}	code block delimiters	Yes	
$\leftrightarrow$	type specialisation	No	New
(	open delimiter	Yes	
)	close delimiter	Yes	
[]	array index delimiters, bit selection	Yes	Array index may be variable
[:]	bit range selection	No	Extended
!	logical NOT operator	Yes	
!	output to channel	No	
$\sim$	bitwise NOT	Yes	
+	addition operator	Yes	
-	subtraction operator	Yes	
-	unary minus operator	Yes	
*	multiplication operator	Yes	
/	division operator	Yes	Extended
%	modulus operator	Yes	Extended
\	drop LSB	No	
$\leftarrow$	take LSBs	No	
?	read from channel	No	
?	conditional expression	Yes	
$\wedge$	Bitwise XOR	Yes	
$\&$	Bitwise AND	Yes	
$\mid$	Bitwise OR	Yes	

FIG. 86A

Keyword	Meaning	ISO-C	New in version 3
&&	Logical AND	Yes	
	Logical OR	Yes	
.	structure member operator	Yes	New
<<	left-shift operator	Yes	Extended
>>	right shift operator	Yes	Extended
<	less than operator	Yes	
>	greater than operator	Yes	
<=	less or equal operator	Not standard <sup>1</sup>	
>=	greater or equal operator	Not standard <sup>1</sup>	
==	equality operator	Not standard <sup>1</sup>	
!=	inequality operator	Not standard <sup>1</sup>	
++	increment operator	Not standard	
--	decrement operator	Not standard	
+=	assignment operator	Not standard	
-=	assignment operator	Not standard	
*=	assignment operator	Not standard	
/=	assignment operator	Not standard	
%=	assignment operator	Not standard	
<<=	assignment operator	Not standard	
>>=	assignment operator	Not standard	
&=	assignment operator	Not standard	
!=	assignment operator	Not standard	
^=	assignment operator	Not standard	
...>	Reserved. Not valid in Handel-C	C only	
->	structure pointer operator	Yes	New
@	concatenation operator	No	

FIG. 86B

Keyword	Meaning	ISO-C	New in version 3
<b>assert</b>	diagnostic macro to print to stderr	Not standard	New
<b>auto</b>	auto variable	Yes	New
<b>break</b>	immediate exit from code block	Yes	
<b>case</b>	selection within switch	Yes	
<b>chan</b>	define channel variable	No	
<b>chanin</b>	simulator channel in	No	
<b>chanout</b>	simulator channel out	No	
<b>char</b>	8-bit variable	Yes	
<b>clock</b>	define clock	No	
<b>const</b>	specify that variable's value will not change	Yes	New
<b>continue</b>	force next iteration of loop	Yes	New
<b>default</b>	default case within switch, prior to	Yes	
<b>delay</b>	wait one clock tick	No	
<b>do</b>	start do while loop	Yes	
<b>double</b>	Reserved. Not valid in Handel-C	C-only	
<b>else</b>	conditional execution	Yes	
<b>enum</b>	enumeration constant	Yes	New
<b>expr</b>	define macro as expression	No	
<b>extern</b>	define global variable	Yes	New
<b>external</b>	clock from device pin	No	Extended
<b>external_divide</b>	clock from device pin with integer division	No	Extended
<b>family</b>	define target device's family	No	
<b>float</b>	Reserved. Not valid in Handel-C	C-only	
<b>for</b>	for loop iteration	Yes	
<b>goto</b>	jump to specified label	Yes	New
<b>if</b>	conditional execution	Yes	
<b>ifselect</b>	conditional compilation on compile-time selection	No	New
<b>in</b>	define scope for local macro expression declaration	No	New
<b>inline</b>	declaration of inline function	No	New

FIG. 86C

Keyword	Meaning	ISO-C	New in version 3
<b>int</b>	definable width variable	Yes	
<b>interface</b>	<b>declaration of off-chip interface</b>	No	Extended
<b>internal</b>	<b>use internal clock</b>	No	Extended
<b>internal_divide</b>	<b>internal clock with integer division</b>	No	Extended
<b>intwidth</b>	<b>set integer width</b>	No	
<b>let</b>	<b>start declaration of local macro expression</b>	No	New
<b>long</b>	declare 32-bit variable	Yes	
<b>macro</b>	<b>declare a macro</b>	No	
<b>mpram</b>	<b>declare a multi-port RAM</b>	No	New
<b>par</b>	<b>execute statements in parallel</b>	No	Extended
<b>part</b>	<b>define target hardware</b>	No	
<b>prialt</b>	<b>execute first ready channel</b>	No	
<b>proc</b>	<b>define macro as procedure</b>	No	
<b>ram</b>	<b>declare a RAM (array)</b>	No	
<b>register</b>	<b>declare register variable</b>	Yes	New
<b>return</b>	return from function	Yes	New
<b>rom</b>	<b>declare a ROM (array)</b>	No	
<b>select</b>	<b>select expression or macro expr at compile time</b>	No	
<b>set</b>	<b>specify int width, target or clock</b>	No	
<b>seq</b>	<b>execute statements in sequence</b>	No	New
<b>shared</b>	<b>declare a shared expression</b>	No	
<b>short</b>	declare 16-bit variable	Yes	
<b>signal</b>	<b>declare a signal object</b>	No	New
<b>signed</b>	declare a signed variable	Yes	New
<b>sizeof</b>			
<b>sizeof</b>	Reserved. Not valid in Handel-C	Yes	
<b>static</b>	specify variable with limited scope	Yes	New
<b>struct</b>	declare a structure variable	Yes	New
<b>switch</b>	switch statement (between cases)	Yes	
<b>typedef</b>	define type	Yes	New
<b>typeof</b>	<b>return type of operator</b>	No	New

FIG. 86D

8600

Keyword	Meaning	ISO-C	New in version 3
<b>undefined</b>	<b>specify a variable of undefined width</b>	No	
<b>union</b>			
<b>unsigned</b>	declare an unsigned variable	Yes	
<b>void</b>	specify void return type,	Yes	New
<b>volatile</b>	declare volatile variable	Yes	New
<b>while</b>	loop statement	Yes	
<b>width</b>	<b>return integer width</b>	No	
<b>with</b>	<b>specify interface, signals, channels, ram and rom types, variables etc.</b>	No	
<b>wom</b>	declare a WOM (array)	No	New

**FIG. 86E**

8700

Escape Code	ASCII Value	Meaning
\a	7	Bell (alert)
\b	8	Backspace
\f	12	Form feed
\t	9	Horizontal tab
\n	10	Newline
\v	11	Vertical tab
\r	13	Carriage return
\"	-	Double quote mark
\0	0	String terminator
\\\	-	Backslash
\'	-	Single quote mark
\?	-	Question mark

**FIG. 87A**

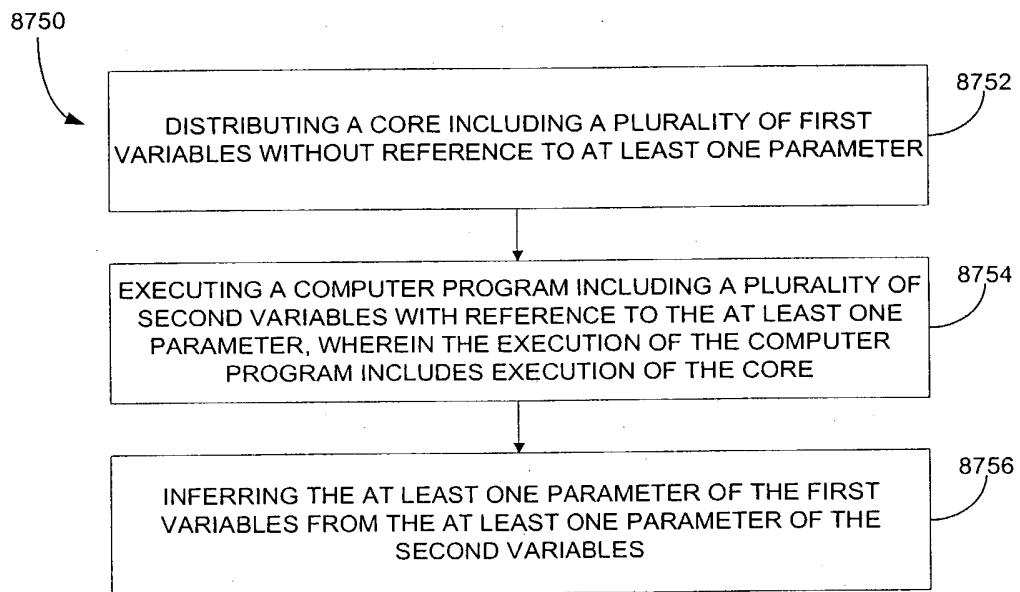


Fig. 87B

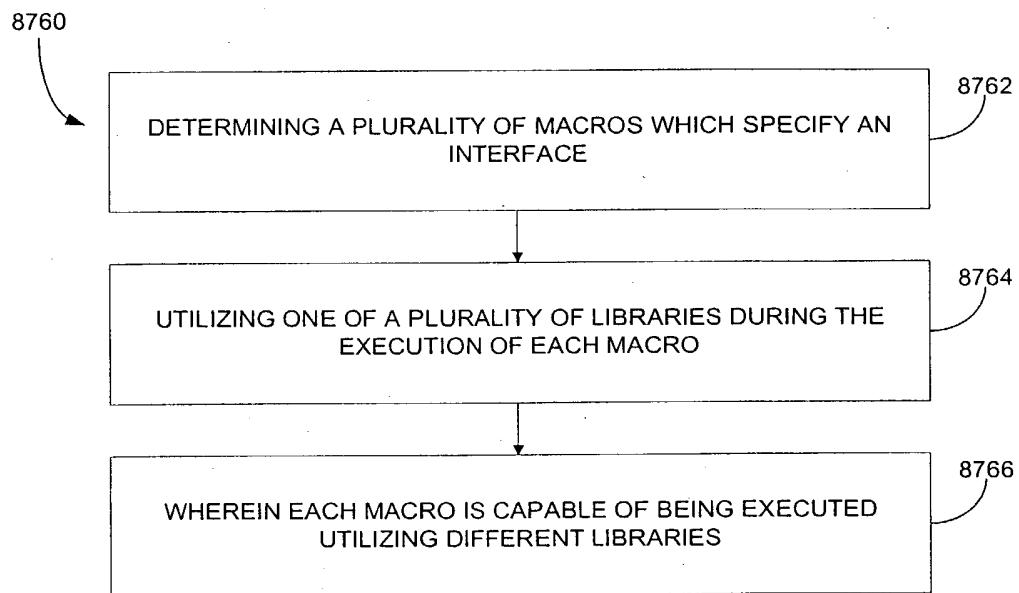


Fig. 87C

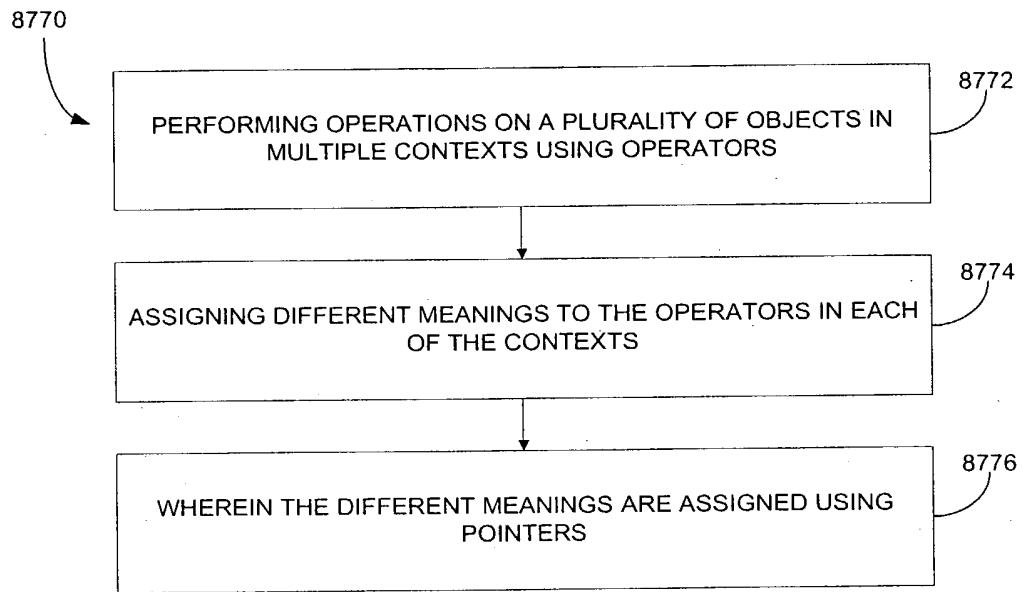


Fig. 87D

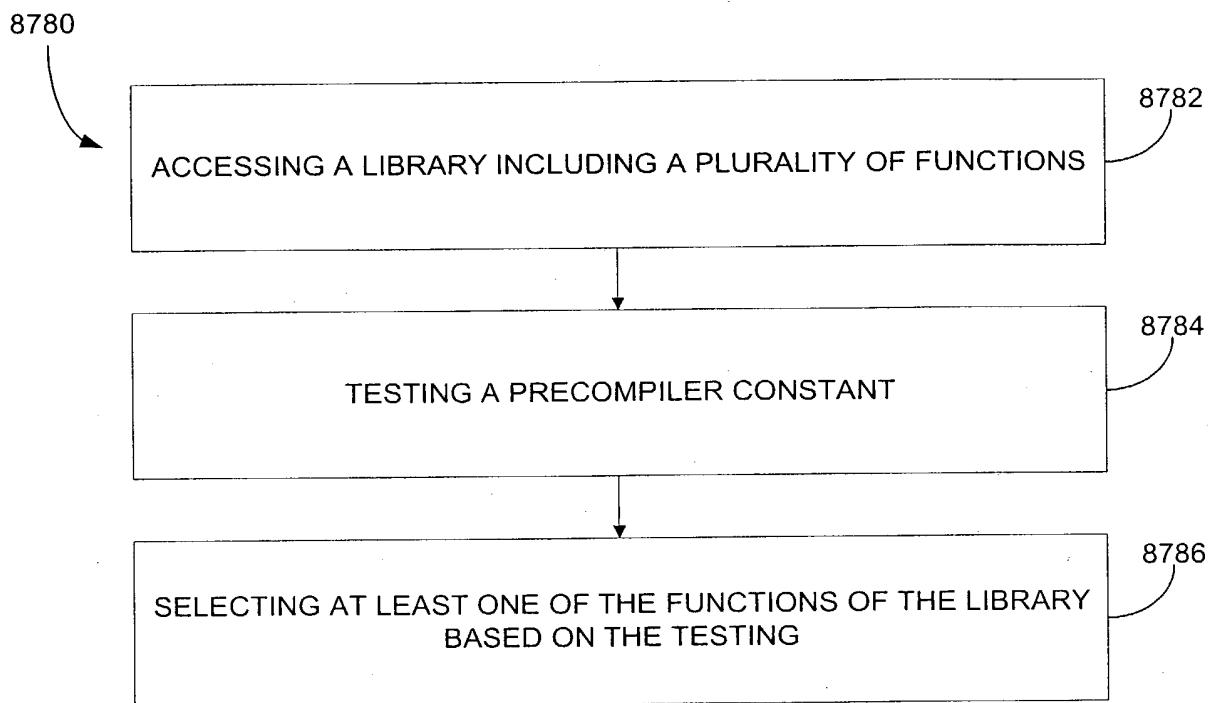


Fig. 87E

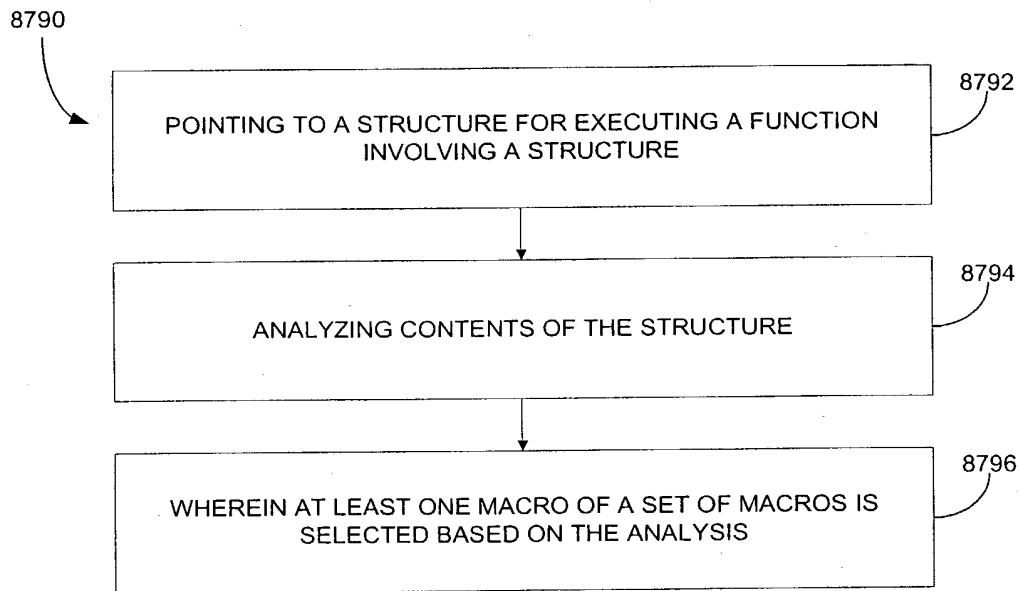
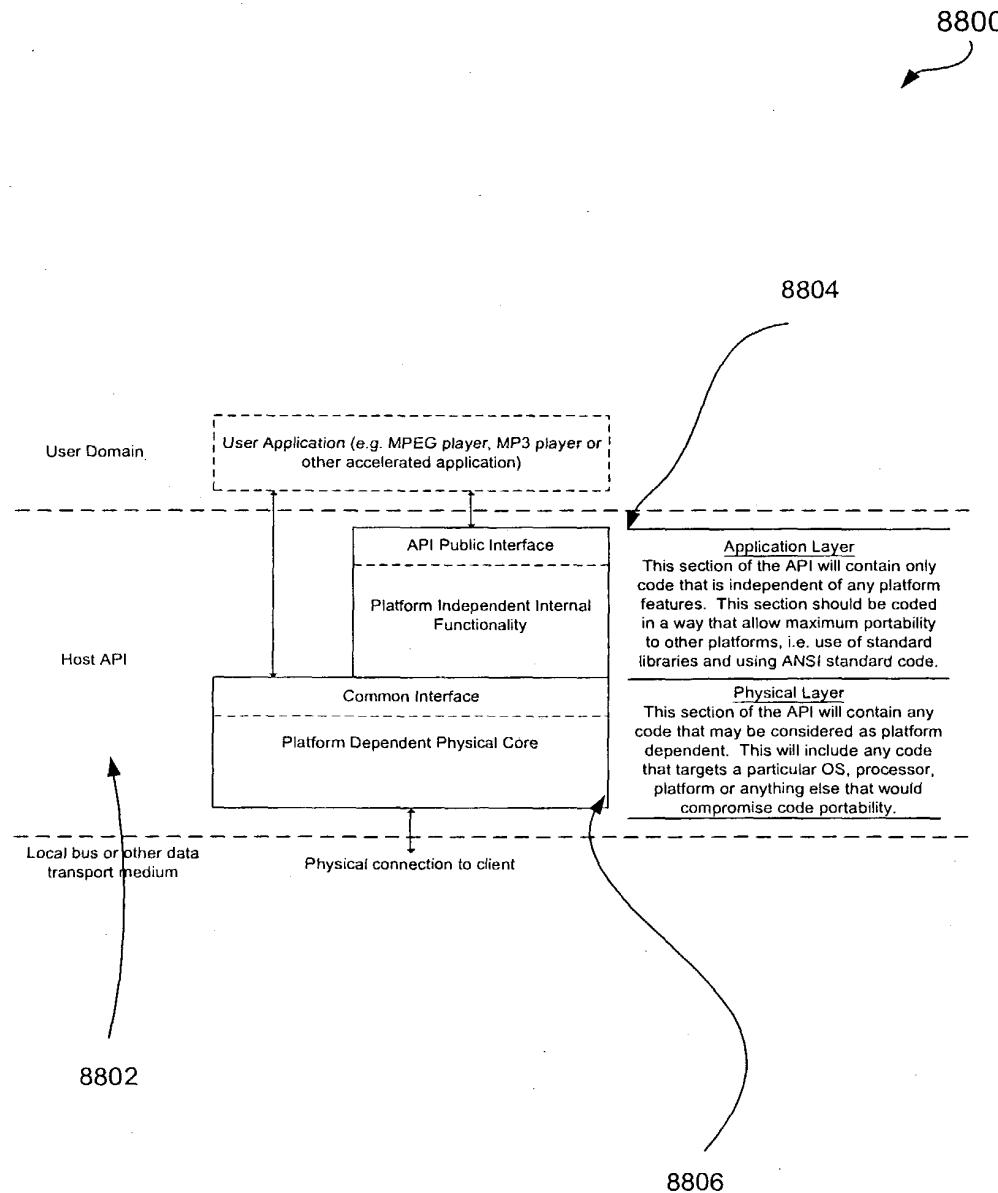
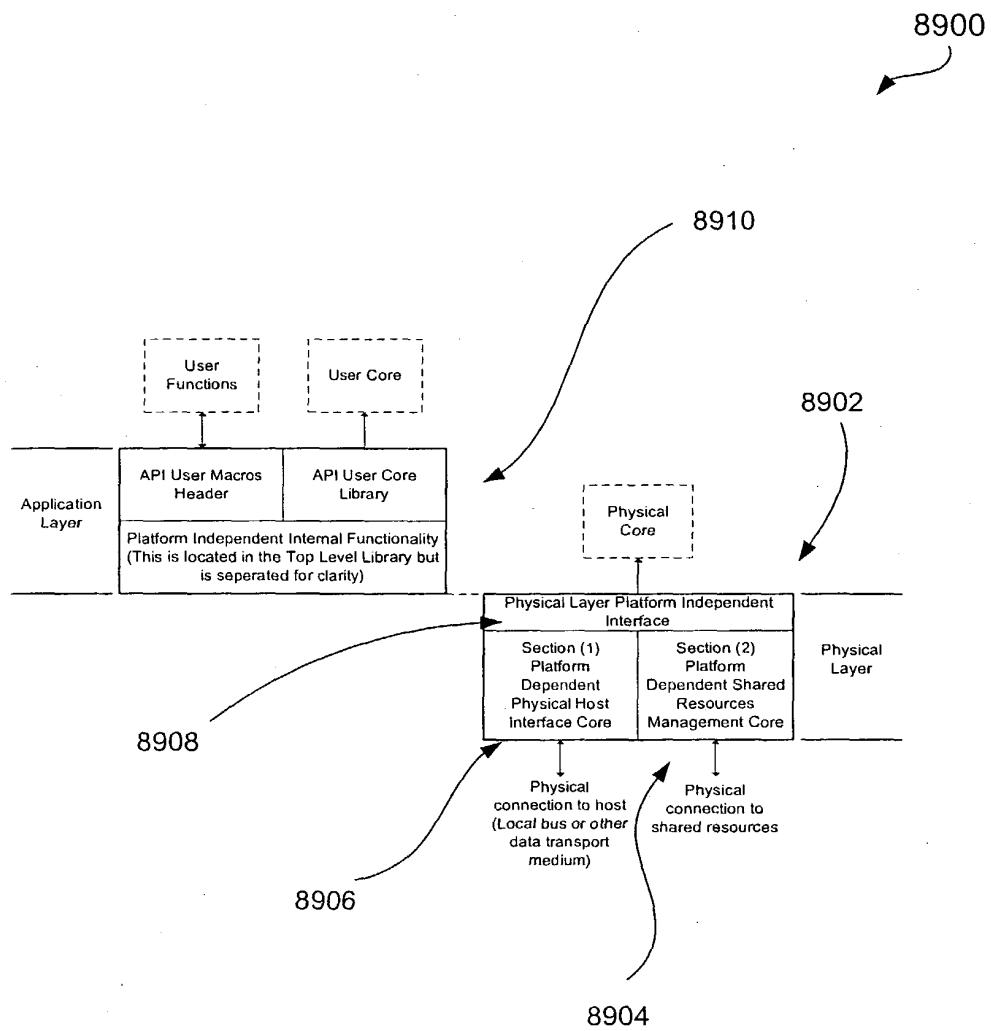


Fig. 87F



**FIG. 88**



**FIG. 89**

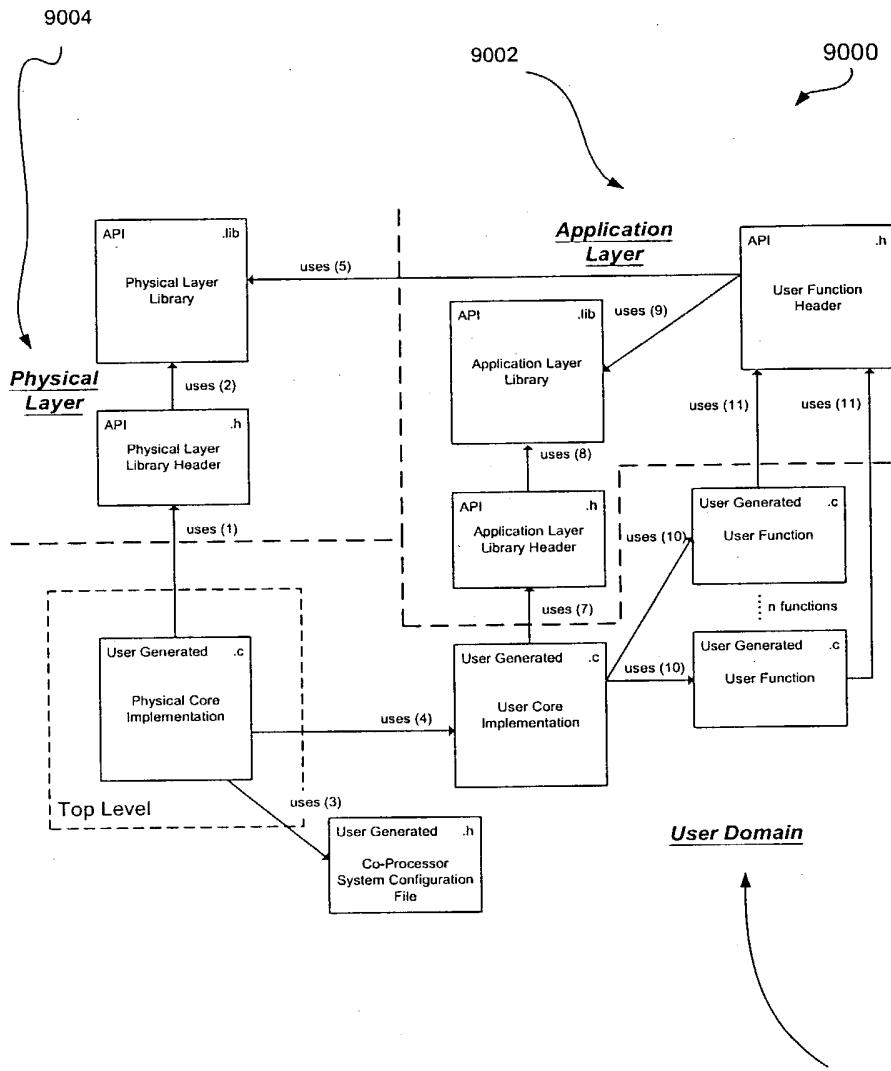
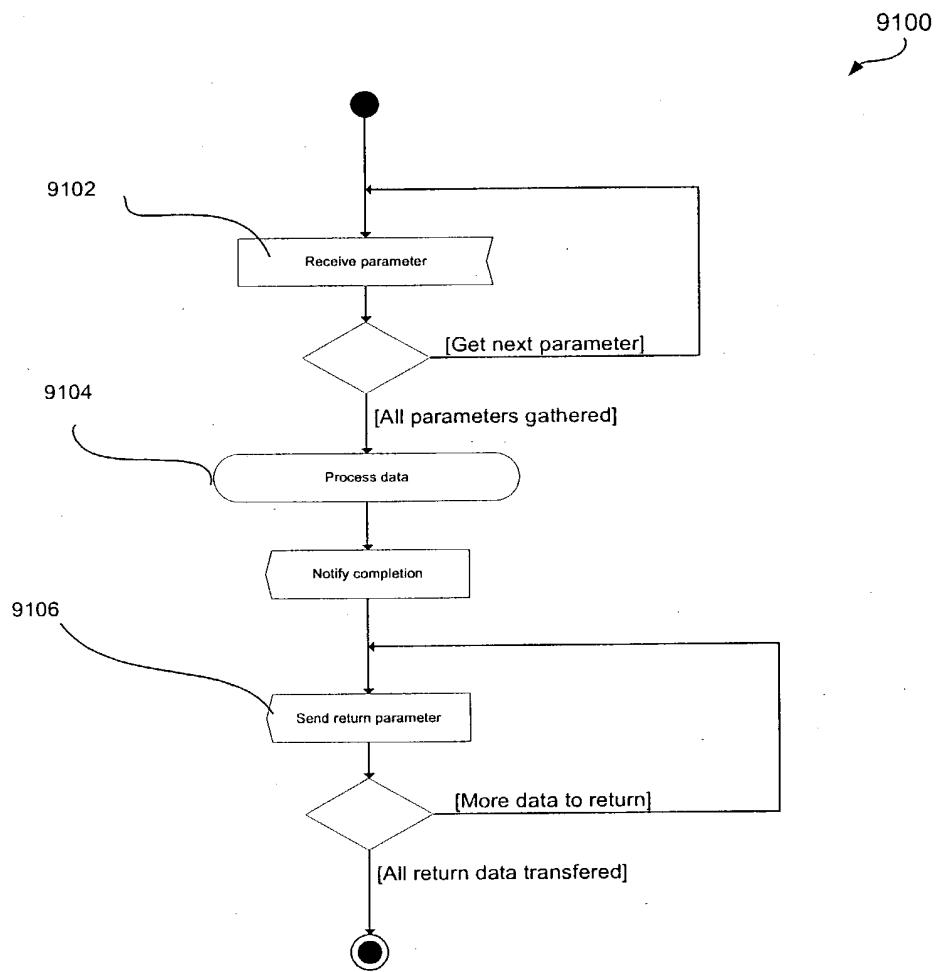


FIG. 90



**FIG. 91**

9200

Typical Address Packet

Address Modifier (8 bits)	Address Index (24 bits)
------------------------------	----------------------------

**FIG. 92**

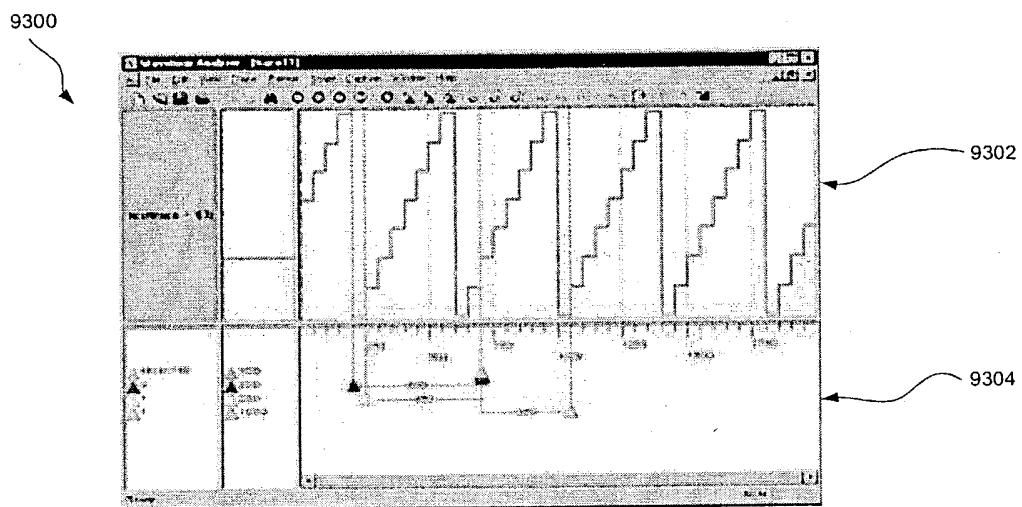


Fig. 93

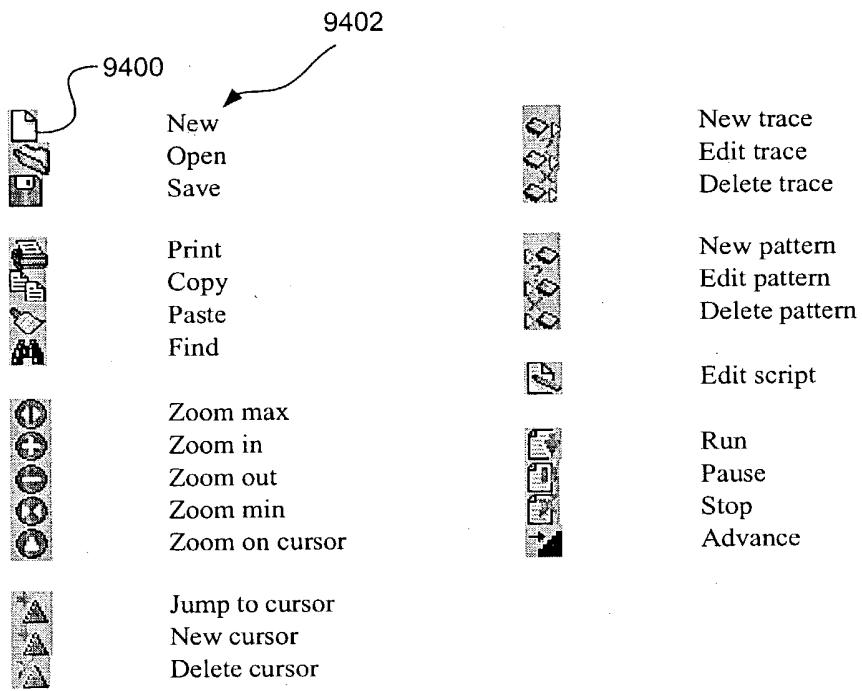


Fig. 94